Nanocrystals for Nanodot Memories - Ion Beam Synthesis and Electrical Studies

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Abstract

The nanodot memory is an emerging non-volatile memory device concept where isolated nanocrystals are used as charge storage nodes instead of a classical poly-Si floating gate. As a combination of ion implantation and subsequent annealing, the versatile method of ion beam synthesis is used in this thesis to prepare tiny Ge and Si nanocrystals in very thin gate oxides. During the thermal treatment after Ge^+ implantation an enhanced diffusion of Ge in the oxide is obtained which leads to a considerable Ge redistribution as well as to a partial loss of the implanted Ge. Both effects were studied in detail including a model of Ge diffusion in SiO_2. Due to a self-organizing process, a narrow layer of Ge nanocrystals forms in SiO_2 in vicinity to the Si substrate which is a desired configuration for nanodot memory devices. Metal-oxide-semiconductor capacitor devices were prepared to study the electrical characteristics of the Ge and Si nanocrystal containing gate oxides by means of capacitance-voltage and current-voltage measurements. Additionally, in this thesis a transient electrical model was developed to describe the charging characteristics of such devices as a function of the programming voltage pulse height and duration with respect to the tunneling oxide thickness, nanocrystal size and density. Based on this model, for the first time the statistics of the individual tunneling distances between the nanocrystals and the Si substrate were obtained from simple programming characteristics. For Si and Ge implanted gate oxides leakage current characteristics were calculated with convincing agreements to the current-voltage measurements. It is shown that the leakage current depends mainly on the location of the nanocrystals in the gate oxides and not on implantation related oxide defects. The structural information needed for all these investigations were deduced from energy filtered transmission electron micrographs and Rutherford backscattering spectrometry.

Kurzfassung

Der Nanodot-Speicher gehört gegenwärtig zu den meist diskutiertesten Konzepten für zukünftige nicht-flüchtige Speicherbauelemente. Dabei werden statt eines poly-Silizium "Floating Gates" isolierte Nanokristalle zur Ladungsspeicherung verwendet. Für diese Dissertationsarbeit wurden in sehr dünnen Gateoxiden winzige Ge und Si Nanokristalle mittels Ionenstrahlsynthese hergestellt, einer Kombination aus Ionenimplantation und anschliessender Ausheilung. Während der thermischen Behandlung nach der Ge^+ Implantation wurde im Oxid eine erhöhte Diffusion des Germaniums beobachtet, welche sowohl eine Umverteilung des Ge auch einen teilweisen Verlust des implantierten Germaniums zur Folge hatte. Beide Effekte wurden im Detail untersucht und ein Modell für die Ge-Diffusion in SiO_2 aufgestellt. Ein selbst-organisierender Prozess sorgt dafür, dass sich Ge Nanokristallen vorwiegend in einem eng begrenzten Bereich im Oxid nahe des Si Substrates - eine gewünschte Anordnung für Nanodot-Speicherbauelemente - formieren. Metall-Oxid-Halbleiter Kapazitätsbauelemente wurden hergestellt, um die elektrischen Eigenschaften der Ge- und Si-haltigen Gateoxide mittels Kapazitäts-Spannungs- und Strom-Spannungs-Messungen untersuchen zu können. Zudem wurde in dieser Arbeit ein elektrisches Modell zur Beschreibung des transienten Beladeverhaltens der Baulemente entwickelt unter Berücksichtigung der Höhe und Dauer der Programmierspannungspulse. Insbesondere die Abhängigkeiten von der Tunneloxiddicke, sowie der Größe und Flächendichte der Nanokristalle konnten damit untersucht werden. Basierend auf diesem Modell konnte zum ersten Mal die statistische Verteilung individueller Tunneldistanzen zwischen den Nanokristallen und dem Si Substrat analysiert werden und zwar aus dem Verhalten einfacher Programmierkennlinien. Darüber hinaus wurden für die Si und Ge implantierten Gateoxide Leckstrom-Charakteristika berechnet, die überzeugende Übereinstimmungen mit den gemessenen Strom-Spannungskennlinien aufweisen. Dabei konnte gezeigt werden, dass der Leckstrom im Wesentlichen durch den Ort der Nanokristalle im Oxid definiert ist und nicht durch implantationsbedingte Oxiddefekte. Die benötigten strukturellen Informationen wurden mittels energiegefilterter Transmissionselektronenmikroskopie und Rutherford-Rückstreu-Spektrometrie erlangt.

Schlagworte: Ionenimplantation, Nanokristalle, nichtflüchtige Speicherbauelmente

Keywords: ion implantation, nanocrystals, non-volatile memory

List of publications and thesis conception

In this thesis the major results are summarized in five previously published or submitted manuscripts to refereed journals which are included in this work as separate chapters (chapter 5 - 9). These papers are printed in the format of publication or in a similar two-column paper-like style.

- ☞ V. Beyer and J. v. Borany *Elemental redistribution and Ge loss during ion-beam synthesis of Ge nanocrystals in SiO_2 films.* Phys. Rev. B, 014107 (2008) (chapter 5)
- ☞ V. Beyer, J. v. Borany, and M. Klimenkov *A transient electrical model of charging for Ge nanocrystal containing gate oxides.* J. Appl. Phys. 101, 094507 (2007) (chapter 6)
- ☞ V. Beyer, J. v. Borany, and M. Klimenkov *Determination and evolution of tunneling distances in Ge nanocrystal based memories* Appl. Phys. Lett. 89, 193505 (2006) (chapter 7)
- ☞ V. Beyer, J. v. Borany, M. Klimenkov, and T. Müller *Current-voltage characteristics of metal-oxide-semiconductor devices containing Ge or Si nanocrystals in thin gate oxides.* accepted for publication in J. Appl. Phys. (2009) (chapter 8)
- ☞ V. Beyer, J. v. Borany, and K.-H. Heinig *Dissociation of Si^+ ion implanted and as-grown thin SiO_2 layers during annealing in ultra-pure neutral ambient by emanation of SiO.* J. Appl. Phys. 101, 053516 (2007) (chapter 9)

As a contribution to a book an article has been previously published by Springer-Verlag, Berlin which discusses the different concepts and recent progresses in the subject of ion beam synthesis of Si and Ge nanocrystals in thin gate oxides for memory device applications.

- ☞ V. Beyer and J. v. Borany *Ion-beam Synthesis of Nanocrystals for Multidot Memory Structures* in: Materials for Information Technology, edited by E. Zschech, C. Whelan, and T. Mikolajick (Springer Verlag, Berlin), pp. 139-147 (2005)

List of Acronyms and Abbreviations

ALD	atomic layer deposition
CHE	channel hot electron
CMOS	complementary MOS
C-V	capacitance-voltage
CVD	chemical vapor deposition
DT	direct tunneling
DRAM	dynamic random access memory
EELS	electron energy loss spectroscopy
EEPROM	electrically erasable and programmable read only memory
EFTEM	energy filtered TEM
F-N	Fowler Nordheim
HAADF	high-angle annular dark field
IBS	ion beam synthesis
II	ion implantation
ITRS	international technology roadmap for semiconductors
I-V	current-voltage
KLMC	kinetic lattice Monte Carlo
LE	low energy
LPCVD	low-pressure CVD
MONOS	SONOS with metal gate
MOS	metal oxide semiconductor
MOSFET	MOS field effect transistor

NC	nanocrystal
NRA	nuclear reaction analysis
NROM	nitrided read only memory
NVM	non-volatile memory
PCRAM	phase change random access memory
RBS	Rutherford backscattering spectrometry
RTA	rapid thermal annealing
SILC	stress induced leakage current
SONOS	silicon oxide nitride oxide silicon
SRIM	stopping and range of ions in matter
STEM	scanning transmission electron microscopy
TEM	transmission electron microscopy
ToF-SIMS	time of flight secondary ion mass spectrometry
TRIDYN	SRIM simulation code including dynamic composition changes
TXRF	total reflection X-ray fluorescence
ULE	ultra low energy
XPS	X-ray photoelectron spectroscopy

Contents

1 The nanocrystal-based memory device

1.1 Introduction

Semiconductor Si and Ge nanocrystals (NC's) are very promising materials in silicon based memory and optoelectronic technologies fully compatible to modern complementary metal oxide semiconductor (CMOS) processing. In the mid 1990s Tiwari *et al.* introduced a Si NC based memory device with an auspicious performance [1]. Band-to-band recombination of confined excitons in the NC's yields a near-infrared luminescence which is much more efficient than that of bulk silicon (internal photoluminescence quantum efficiency of about 59% [2]). Due to quantum confinement tiny Si NC's (typically of 1 - 4 nm diameter) show also a size tunable electronic bandgap with the option of light emission or absorption at different wavelengths. Thus, the expectable optical applications of Si quantum dots span from Si NC based laser devices [3, 4] to a new generation of photovoltaic solar cells [5]. Very promising, recently, a field-effect electroluminescence in silicon nanocrystals has been demonstrated [6, 7].

In the past decades dramatic improvements have been achieved in the silicon technology and the related device performances. In 1965 Gordon E. Moore predicted that the complexity (the number of transistors in an integrated circuit) increases roughly with a factor of two per year [8], which was refined in 1975 to a period of two years. Since that time this rule - called "Moore's law" - has a self-fulfilling prophecy as the entire microelectronic industry adapted this as a goal for their product and engineering roadmap. The **I**nternational **T**echnology **R**oadmap for **S**emiconductors (ITRS), which documents the current technology standards, uses this law to predict the device performances and technology demands for about the next 15 years [9]. Actually, one of the most difficult challenges for emerging research devices is attributed to the development of an electrically accessible high speed and high density non-volatile memory. It was found that the most limiting factor to increase the microprocessor program executing performance is the slow access to external storage media, e.g. to magnetic hard drives. A nanoscale non-volatile memory device is thought to improve the information throughput significantly, with the potential to "initiate a revolution in computer architecture" [9]. According to the actual roadmap there are two most promising candidates of emerging memory devices [9]. The nanofloating gate device includes all concepts which utilize a charge storage in discrete traps; the nanocrystal (also known as nanodot or multidot) memory depends to this type. The other concept considers a floating gate device with an engineered (graded or "crested") tunnel barrier with the consequence of the introduction of new tunnel oxide

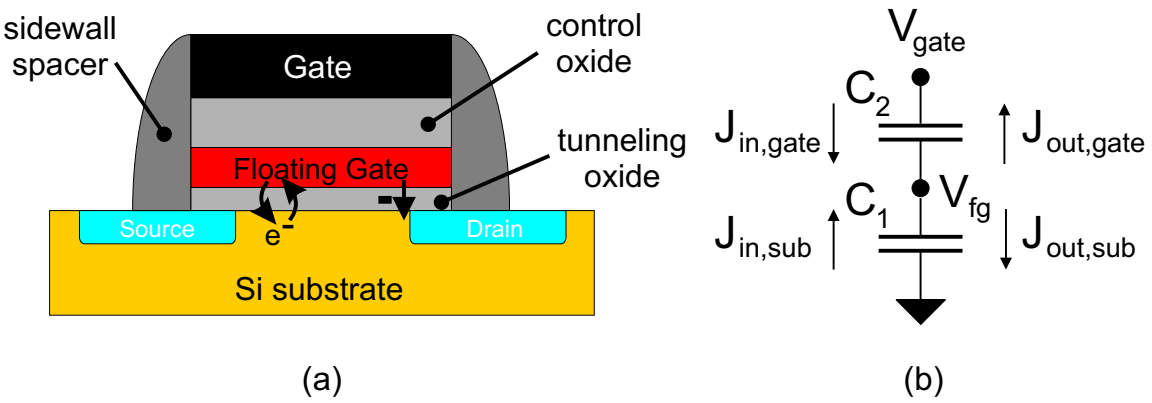


Figure 1.1: (a) Schematic of an EEPROM non-volatile memory transistor cell in cross-sectional view. Programming and erasing occurs due to a charge exchange between the floating gate and the Si substrate across the tunneling oxide. A single leakage path through this oxide induces a complete discharge of the floating gate and, thus, complete data loss. (b) Simplified capacitor model of a floating gate memory device.

materials like Al_2O_3 or HfO_2 (see the following sections and Fig. 1.8 for details).

This thesis is aiming at nanocrystal memory devices and their electrical characteristics, whereas the Si (and Ge) nanocrystals are synthesized in 20 nm thin gate oxides by ion implantation and subsequent annealing. Both processes used in ion beam synthesis are widely accepted in the microelectronic industries, they are well-known and cost-effective.

1.2 Basics of non-volatile memory devices

The most popular form of a conventional non-volatile memory is the **E**lectrically **E**rasable and **P**rogrammable **R**ead-**O**nly **M**emory (EEPROM). As schematically shown in Fig. 1.1, this device consists of an isolated highly doped poly-Si layer, called floating gate, embedded in the gate oxide of a metal-oxide-semiconductor (MOS) field effect transistor (FET) [10]. An alternative is the **s**ilicon-**o**xide-**n**itride-**o**xide-**s**ilicon (SONOS) memory device where the poly-Si floating gate is exchanged by a charge trapping Si_3N_4 layer [see Fig. 1.2(b)] [10]. In modern data storage devices like memory cards, USB sticks, or solid state drives, we find floating gate devices integrated in a Flash memory architecture which implies block-wise erase at once. Electrons, which are injected from the Si substrate (the Si channel) into the floating gate by **F**owler-**N**ordheim (F-N) tunneling or channel-hot-electron (CHE) injection, cause a shift of the threshold voltage of the transistor which is analyzed sensing the source-drain current (for details see Ref. [10]). The most relevant parameters to evaluate the performance of a single memory transistor cell are [10]

- the **programming characteristics** which shows the shifting of the threshold voltage as a function of the applied programming voltage and time;
- the **device retention** indicating the ability to retain the stored charge as a function

of the storage time (> 10 years are required for real non-volatility);

- the **endurance characteristics** revealing the memory device reliability as a function of the number of applied write/erase cycles. EEPROM cells hold typically 10^6 cycles without significant changes in the threshold voltages in the programmed or erased states.

An overview of Flash memory cells and their basic principles is given in Refs. [10], [11]. Disregarding the source and drain contacts to reduce the memory transistor to a **m**etal-**o**xide-**s**emiconductor (MOS) capacitor device, the potential of the floating gate (V_{fg}) simplifies to

$$V_{fg} = \frac{C_2}{C_1 + C_2} V_{gate} + \frac{Q_{fg}}{C_1 + C_2} \tag{1.1}$$

with the capacitances of the tunneling and control oxide C_1 and C_2 (in units of $\mathrm{F}/\,\mathrm{cm}^2$), respectively [see Fig. 1.1(b)]. V_{gate} is the potential of the gate with respect to the Si substrate. The charge density stored at the floating gate Q_{fg} changes with time t as electrons or hole are transferred through the tunneling or control oxide contributing to the positive or negative current density J_i in Eq. (1.2).

$$Q_{fg}(t) = \int_0^t \sum_{A_i} J_i[E_i(t)]dt \tag{1.2}$$

A_i subsume all areas of charge injection (or ejection) toward (or from) the floating gate. The electrical fields E_i across the tunneling and control oxides are themselves a function of V_{cg} and Q_{fg} implicitly [10]. As a consequence, Eq. (1.2) can not be solved directly. One way to handle this problem is to calculate the internal potentials and the amount of charges numerically solving this equation iteratively as a function of the programming time, for instance, with very small time increments. Discussing the data retention of a Flash memory device usually a temperature activated process is considered for the charge loss following the Arrhenius law (E_A is its activation energy, t_R the retention time, and t_0 the retention time corresponding to an infinite temperature) [12].

$$t_R \;=\; t_0\, e^{E_A/kT} \tag{1.3}$$

As mentioned by De Salvo *et al.* [12] the measured EEPROM retention data loss characteristic has an exponential temperature dependence with T and not with $1/T$ as predicted by Eq. (1.3). This behavior is explained by the temperature dependence of the Fowler-Nordheim tunneling current which is the dominant charge loss mechanism in classical floating gate devices.

The conventional floating gate memory device suffers mainly from its sensitivity to oxide defects. A single defect or trap within the tunneling oxide can open leakage paths to deplete the floating gate leading to a complete data loss and memory device failure. Such defects are, for instance, generated during write/erase cycling, i.e. electron in-/ejection at high electrical fields across the tunneling oxide, which results in the so called "**s**tress **i**nduced **l**eakage **c**urrents" (SILC) [13]. As the performance of such a classical floating

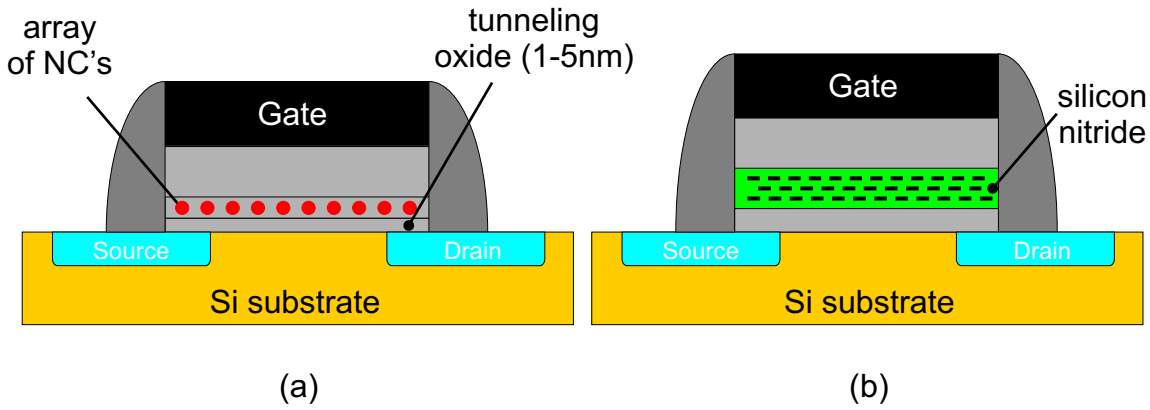


Figure 1.2: Different charge trapping non-volatile memory concepts, the nanocrystal-based (a) and SONOS memory device (b). In both cases the charge is trapped at individual storage nodes, at nanocrytals (a) or natural silicon-nitride traps (b).

gate memory device depends crucially on the quality of the tunneling oxide, an oxide thickness of at least 7 nm is needed to ensure real non-volatility. As a consequence, the conventional Flash EEPROM still suffers from high programming voltages (e.g. $\geq$ 15 V) resulting in high electrical oxide fields during write-/erase operation and, thus, hot-carrier degradation of the tunneling oxide limiting the retention and endurance memory device performance. This contradicts to design rules for further device scaling to achieve higher data densities where the shrinking of the transistor dimensions also includes a decreasing tunneling oxide thickness.

1.3 Nanocrystal memory device characteristics

In the mid 1990s Tiwari *et al.* [1, 14] proposed a nanocrystal based memory device to overcome expectable limitations for the conventional non-volatile memory device concepts (oxide thickness scalability, operation at lower voltages, power consumption, write/erase speed etc.). As the most prominent approach for the nano-floating gate memories - according to the actual International Technology Roadmap for Semiconductors (ITRS) [9] - this topic has dominated the research activities of emerging memory devices over the past 10 years (Fig. 1.8). The nanocrystal memory has an outstanding advantage over other memory concepts (e.g. magnetic or ferroelectric memories) as it is easily integratable in conventional silicon technology and CMOS processing. As shown in Fig. 1.2(a) in such a device the floating gate is replaced by a layer of tiny (much smaller than 10 nm in diameter) semiconductor (Si, Ge) nanocrystals embedded in SiO_2 well separated from each other and the Si/SiO_2 interface. In Fig. 1.3 its working principle is illustrated. Charges are transferred from the Si substrate into three-dimensionally confined nanocrystals by a direct tunneling mechanism, which promises fast operation at room temperature at low gate voltages and low power consumption [1]. These charges stored within the gate oxide of the transistor cause a shift of the onset characteristic which can also be traced on MOS

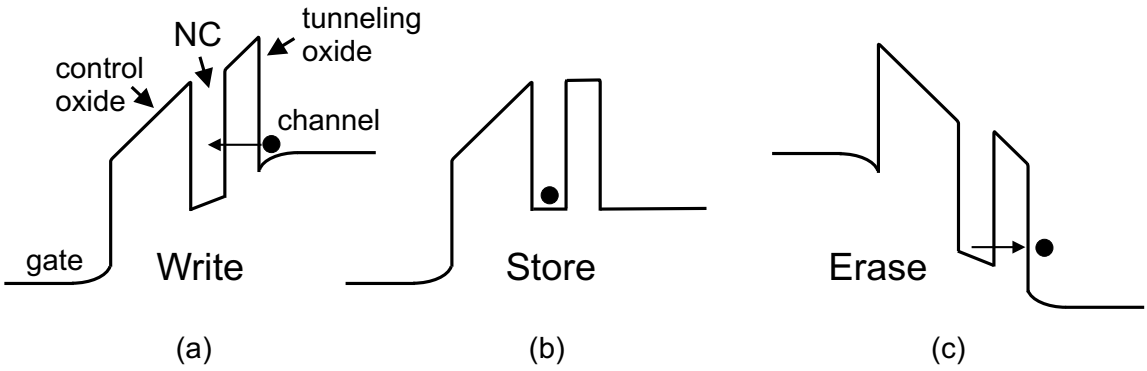


Figure 1.3: Schematic band diagram of write, store and erase operations (a-c) for charge storage in a nanocrystals containing memory device after Ref. [1].

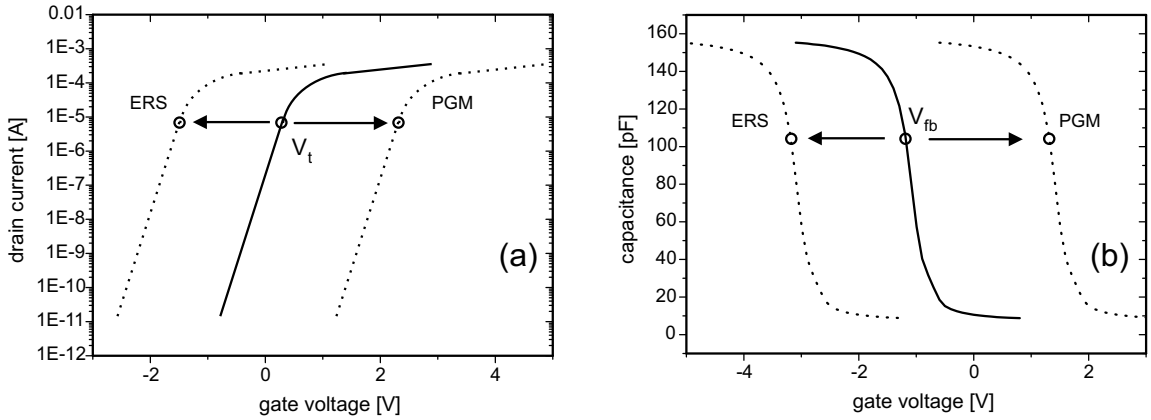


Figure 1.4: Shifting of (a) the subthreshold I-V characteristic of a memory n-FET transistor or (b) the C-V characteristic of a NC containing MOS capacitor device demonstrating schematically the initial, the programmed (PGM), and erased state (ERS) of the device.

capacitor devices (see Fig. 1.4). Due to an isolating spacing between the nanocrystals, a charge dispersion within this layer is suppressed and, thus, also a complete spontaneous charge loss through a single oxide leakage path to the substrate is avoided. This enables a low voltage operation with direct tunneling through a thinner oxide layer ($d_{ox} < 5\,\mathrm{nm}$) where high electrical fields with hot-carrier oxide degradation are not necessary anymore [1]. Thus, the charge storage in nanocrystals instead of in a conventional floating gate offers several attractive advantages:

- **fast write and erase processes** become possible due to large current densities in the direct tunneling regime,
- avoidance of hot carriers enables **an extremely reduced oxide degradation** in comparison to conventional Flash or nitride trapping devices (SONOS),
- **operation at smaller voltages** in the direct tunneling regime with **lower power consumption** than EEPROMs

- with the perspective of **acceptable retention time and also non-volatility**,
- in combination with a **simple fabrication process** and therefore **low costs**.

As this device is usually numerously embedded in NOR or NAND architectures also additional advantages appear, e.g., a decreased floating-gate capacitance coupling or suppression of "erratic bits" and drain-turn phenomena (see Ref. [15] for details).

The magnitude of the threshold shift ΔV_t, which separates the programmed "1" or erased "0" state of the device from the initially uncharged state, is approximately given by

$$\Delta V_t = \frac{nqN_{nc}}{\varepsilon_{ox}} \left(d_{cox} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{nc}} d_{nc} \right) \quad . \tag{1.4}$$

There, n represents the averaged number of charges per nanocrystal and q the electron's charge. ε_{ox} and ε_{nc} are the dielectric constants of the oxide (usually SiO_2) and the NC's, respectively. A similar equation [Eq.(4.7)] describes the shift of the flatband voltage V_{fb} of the C-V characteristic of a MOS capacitor device (see also Fig. 1.4). Considering a mono-dispersed array ($N_{nc} = 3{\times}10^{12}\,\mathrm{cm}^{-2}$) of Ge nanocrystals embedded in SiO_2 ($d_{nc} = 2\,\mathrm{nm}$) as shown in Fig. 1.2(a), a considerable threshold voltage shift of about 2 V is achieved assuming one stored charge per nanocrystal and a typical control oxide thickness d_{cox} of 15 nm ($\varepsilon_{nc} = 16\,\varepsilon_0$, ε_0 is the permittivity of free space [16]). A key parameter of the nanocrystal memory programming performance is - with experimental evidence [17] - the areal coverage ratio of the nanocrystals R_{nc} and not only the areal dot density N_{nc} as predicted in Eq. (1.4) [18].

$$R_{nc} = A_{nc}/A_{tot} = \frac{\pi}{4} d_{nc}^2 N_{nc} \,<\, 1\,, \tag{1.5}$$

A_{nc} is the projected area of the square NC surfaces and A_{tot} the total device (gate) area. This ratio defines the effective tunneling oxide areal fraction available for nanocrystal charging and is, thus, besides the tunneling oxide thickness and tunneling barrier heights, a key parameter for the programming and erase time performance. As a consequence, the nanocrystal size and density are crucial parameters with respect to NC formation. The scalability of a nanocrystal-based memory device demands a NC density considerably exceeding $N_{nc} = 1{\times}10^{12}\,\mathrm{cm}^{-2}$ in order to ensure a clear separation between the "1" and "0" memory states [19]. Each cell transistor has to contain a sufficient number of NC's without significant deviations in the programming and erase performance from device to device. At the same time charge propagation between the NC's should be inhibited with a minimum inter-nanocrystal distance of about 3 nm, for instance. In any case the distance between the nanocrystals should be larger than the distance to the Si substrate (the tunneling oxide thickness) [20]. In a simple approximation of uniformly distributed, monodispersed nanocrystals in a floating gate layer as shown in the inset of Fig. 1.5, the NC density can be easily deduced by

$$N_{nc} \,=\, \frac{1}{a^2} \,=\, \frac{1}{(\Delta + d_{nc})^{\,2}} \tag{1.6}$$

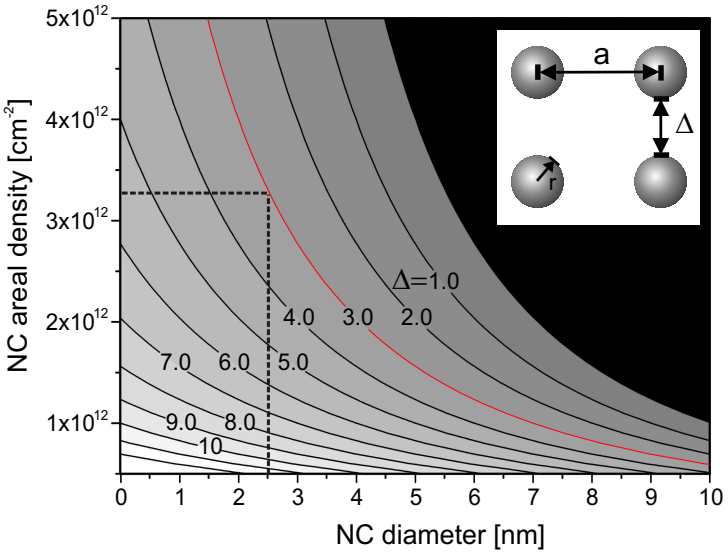


Figure 1.5: Minimum tunneling distance Δ (in nm) as a function of the NC density and size using Eq. (1.6) according to a homogeneous distribution of NC's as illustrated in the inset. The black shaded area represents connected NC's, equivalent to a continuous floating gate. For example, as indicated by the broken lines a layer of regularly distributed NC's of 2.5 nm size with a minimum distance of 3 nm between each other yields a NC density of 3 - $3.5\times10^{12}\,\mathrm{cm}^{-2}$.

for a known NC size d_{nc} and a tunneling distance Δ between two nearest neighbored ones (a is the "lattice constant" of the NC array). As shown in Fig. 1.5 with these assumptions a density of about $3\times10^{12}\,\mathrm{cm}^{-2}$ is only achievable with a NC size of $d_{nc} \leq 3\,\mathrm{nm}$. Thinking about a suitable NC preparation technique, it is an excellence of the ion beam synthesis method to fulfill these demands easily without particular time and money spending efforts.

1.4 Synthesis of nanocrystals and first demonstrated Mbit memory arrays

Numerous efforts have been carried out to prepare Si nanocrystals in host matrices, preferably in a high density. Besides ion beam synthesis [21] - which is the topic of this thesis and discussed in detail in chapter 2 - manifold deposition techniques were reported. An overview is given by De Blauwe [22]. An aerosol technique was investigated [23], chemical vapor deposition (CVD) [24, 25, 26], and also amorphous-Si or Si-rich oxide layer physical vapor deposition (PVD) [27, 28], whereas the NC formation occurs during a recrystallizing annealing treatment. From these methods the CVD provides the best control over size and density of the nanocrystals (details of this method are reported by Rao *et al.* [25]): SiH_4 molecules adsorb on the previously thermally-grown tunneling oxide layer surface and dissociate there building Si adatoms. These atoms work either as

centers to form new nuclei or are consumed by existing and growing NC's by surface diffusion [25]. Usually, the reported nanocrystal density is in the range between $1\times10^{11}\,\mathrm{cm}^{-2}$ and $1\times10^{12}\,\mathrm{cm}^{-2}$ with a mean NC diameter of about 5 nm. The highest dot density ever reached by (low pressure) CVD in the literature is $N_{nc}=2\times10^{12}\,\mathrm{cm}^{-2}$ with a mean dot size of about 3 nm using highly hydroxylated SiO_2 [24]. Also the preparation of Si NC's on alumina was reported, which is important for a future application of NVM devices using high-k materials [29]. Similar and also alternative methods are reported for the formation of Ge NC's in SiO_2, e.g., the Ge or Ge/SiO_2 co-sputtering [30], an oxidation of $Si_{1-x}Ge_x$ layers [31], a reduction of CVD $Si_{0.75}Si_{0.25}O_2$ layers by H_2 [32], molecular beam epitaxy [33], the sol-gel method [34], and also ion implantation [35, 36, 37]. Additionally, a Ge/Si hetero-nanocrystal memory device was discussed [38]. Metal NC's are usually prepared by e-beam evaporation and subsequent annealing (Au, W, Ag, Pt) [39], Au sputtering [40] or via decomposition of sputtered $Au_{0.25}Si_{0.75}$ or W_5Si_3 silicide layers [41, 42]. A double $CoSi_2$ layer was produced by subsequent a-Si/Co/a-Si electron beam evaporation and plasma enhanced CVD [43]. Recently, a hexagonal-ordered array of Co NC's was prepared in a very small size distribution using diblock copolymer micelle templates with embedded Co [44].

Freescale (formerly known as Motorola) launched in 2003 first functional 4-Mbit Si nanocrystal-based non-volatile memory cell arrays and later on also 24-Mbit cell arrays [45]. The memory devices were easily integrated in a standard CMOS flow at low costs (a conventional 90 nm technology process) working at a maximum chip voltage of 6 V with sub-10 μs programming and sub-100 ms erase times [46]. The total memory size was reduced approximately by a factor of two in comparison to a conventional floating gate nonvolatile memory device [46]. The Si nanocrystals were prepared by CVD in an areal density ranging between $5\times10^{11}\,\mathrm{cm}^{-2}$ and $1.1\times10^{12}\,\mathrm{cm}^{-2}$. It should be mentioned that Freescale uses the nanocrystal memory device mainly in automotive applications, which has the most critical and challenging data safety demands [47]. Nitride memory devices, as discussed in chapter 1.7, suffer from the required writing operations using channel-hot electrons with the consequence of an early tunneling oxide wear out. In contrary, nanocrystal memories utilize direct or Fowler Nordheim tunneling processes with a weaker oxide destruction potential.

1.5 Quantum confinement and Coulomb blockade effect

Dealing with particles on nanometer scales quantum size effects have to be taken into account. Contrary to metal NC's, where the valence and conduction bands overlap, semiconductor NC's exhibit a strongly size-dependent energy gap. If the semiconductor nano-particle diameter is below the order of the Bohr exciton (radius of this material), quantum confinement effects become relevant, which leads to an increasing band gap with decreasing particle size [48, 49, 50].

$$E = E_g + \frac{\hbar^2\pi^2}{2r^2}\left[\frac{1}{m_e}+\frac{1}{m_h}\right] - \frac{1.8e^2}{\varepsilon r} + \frac{e^2}{r}\sum_{n=1}^{\infty} a_n \left(\frac{S}{r}\right)^{2n} \tag{1.7}$$

The lowest excited 1s state E (with respect to the bulk bandgap E_g) depends on the electron-hole quantum localization (first term), the Coulomb attraction (second term) and polarization (third term). r is the radius of the nano-particle, m_e and m_h the electron and hole masses, respectively, and h Planck's constant. a_n depends on the dielectric properties of the particle and the host and S is a position variable inside the NC sphere which has the dielectric coefficient ε. Due to quantum confinement the continuum of electronic transitions within the bands splits into separate energy levels. From the Bohr exciton radius in Si and Ge of 4.3 and 24.3 nm [51], respectively, a more pronounced quantum confinement effect can be expected in case of Ge than of Si NC's of 2 - 3 nm size. The analysis of photoluminescence spectra of, e.g., Si NC's [52, 53, 54] gives a hint of the real NC band-gap energy and NC size evolution during annealing due to band-to-band radiative recombination of confined electron-hole pairs [55, 56]. However, to obtain the NC size directly from the luminescence energy is very difficult, because the band-gap energy is also dependent on the kind of NC surface passivation [57, 58]. Considering hydrogen or oxygen bonds at the NC rim, which is likely in case of Ge or Si NC's being embedded in SiO_2, the band-gap widening due to quantum confinement is strongly quenched [57].

The basis of single-electron device concepts in quantum-dot structures, which are embedded in tunnel-junction systems, is the Coulomb blockade effect [59, 60]. Thinking about a room temperature application such phenomena only matter if the classical electrostatic charging energy E_c

$$E_c = \frac{e^2}{2C} \gg kT \tag{1.8}$$

is much higher than the thermal energy (k is the Boltzmann constant and T the temperature). $C = 2\pi\varepsilon r$ is the self-capacitance of a nanocrystal with radius r which is embedded in a matrix with dielectric constant ε. The typical staircase-like current-voltage characteristic derives from a quantization effect in a charging experiment of a single nanodot; an external bias voltage V_b has to be higher than a discrete threshold value of $V_b = e/C$ to charge the dot with another electron [61]. In single Si nanocrystals these coulomb blockade effects were studied by scanning tunneling spectroscopy [62]. Single-electron transistors suitable for low power operation have been demonstrated working at room temperature [63, 64] and also single-electron memory applications were discussed [65, 66, 67, 68]. In multi-nanocrystal memory devices the coulomb blockade effect is utilized to improve the retention time with self-aligned doubly-stacked dots [69] (see also chapter 1.6). However, single electron charging and discharging phenomena were detected even in ultrascaled Si NC memories [70].

1.6 Data retention limitations and concepts of improvement

Nanocrystal memory devices with a tunneling oxide thickness of $d_{tox} \geq 5$ nm, where the programming and erase operations are carried out by Fowler Nordheim tunneling, show

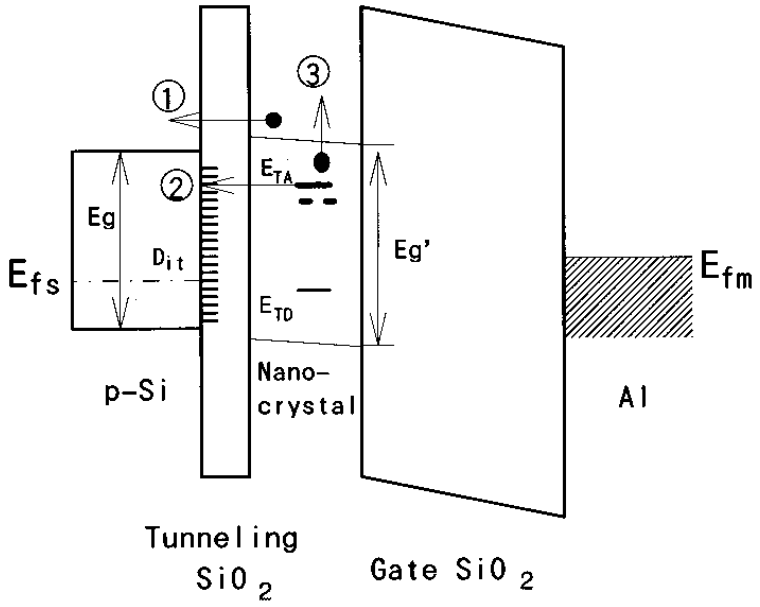


Figure 1.6: A schematic band diagram (taken from Ref. [71]) to illustrate different charge loss mechanisms of a Si NC containing memory structure (①: direct tunneling of electrons from the NC's conduction band to the substrate, ②: direct tunneling of electrons from NC traps to unoccupied states at the Si substrate/SiO_2 interface, ③: thermally detrapping of electrons to the NC conduction band).

real nonvolatile behavior (charge storage up to 10 years) even at a data retention test performed at a high temperature ($T = 250°C$) [15]. The performance of devices, which operate in the direct tunneling regime ($d_{tox} \leq 3.5$ nm), is rather DRAM-like or quasi-(short term)-nonvolatile than real (long term) non-volatile as the data retain only for minutes, hours or days (see Fig. 1.8, for instance). Considering Si NC's as data storage nodes, the electrons are supposed to be stored in the conduction band of the NC. Due to the three-dimensional quantum confinement in the embedded NC's this level is energetically higher than the Si substrate conduction band level. Especially in case of more than one electron stored in the NC's, these electrons can easily tunnel back to the substrate, which is discussed to be the main reason of a short data retention (see process ① in Fig. 1.6) [71]. Considering this "intrinsic" discharging process of a floating-gate like array of nanocrystals a minimum oxide thickness of 4.2 nm is required (for uncycled memories) to guarantee data storage of about 10 years [20]. But, as a trade-off, such a tunneling oxide thickness necessitates longer write times and/or higher programming and erase voltages than those working mainly in the direct tunneling mode. Using Ge instead of Si NC's a long retention time was reported [21], which might be related to the smaller or shifted band gap position of Ge NC's with respect to that of the silicon substrate (see also chapter 6).

Shi *et al.* argued that a long-term data storage at Si NC's is related to charge capture

at traps located at the Si NC/SiO_2 interface [71, 72] (see Fig. 1.6). Due to their energy position the trapped charges see a higher barrier for back-tunneling, which is supposed to improve the data retention [20]. As thermal activated processes were found not to be dominant [72, 73], a mechanism of charge loss via detrapping and direct back-tunneling (processes ③ + ① in Fig. 1.6) seems not to be likely. A long-term charge storage was attributed to a charge loss involving traps located at the Si substrate/tunneling oxide interface (with density D_{it}) as indicated by process ② in Fig. 1.6 [71, 72]. Thus, a low density of interface states there would result in a lower tunneling rate from the NC's to the Si substrate and thus in a longer data retention [72]. But, the quality of this interface is very sensitive to process deviations and stress from device cycling during operation.

Thus, different concepts are discussed to overcome the constrained performance of the "intrinsic" data retention. Likharev [74] introduced the idea to engineer the shape the of the tunneling oxide barrier with a stack of layered barriers using high-k materials like Al_2O_3 or HfO_2. Also self-aligned doubly stack Si dots show an improved charge retention, where a smaller Si dot is located directly below a bigger one [69]: A stronger quantum confinement and Coulomb blockade of the smaller (charged) NC causes an additional energy barrier for charges stored in the upper dot. A similar effect was recently shown for a double layer of $CoSi_2$ NC's [43]. Utilizing the energy difference between the valence band level of the Ge NC's and the Si substrate or NC's, an improved data storage can be expected using Ge NC's instead of Si NC's [21, 75] or Ge/Si hetero-nanocrystals, respectively [38].

Work function engineering is discussed mainly with respect to a replacement of the semiconductor NC's by metal NC's [39]. Metal NC's reveal a variety of barrier heights to the surrounding gate oxide and a well known Fermi energy level due to negligible quantum confinement. In contrary to semiconductor NC's [72], traps at the metal/oxide are supposed to be of subordinate importance, whether due to the high density of states or due to chemical stability of noble metals [76]. For devices containing Au, Ag or Pt NC's operating in the F-N tunneling regime ($d_{tox} = 5\,\mathrm{nm}$) a data retention of up to 10^6 s and also multibit-per-cell storage capability was demonstrated (see chapter 1.7) [77, 78].

1.7 Charge trapping memories, a multibit non-volatile memory cell and new materials

In competition with the classical poly-Si or nanocrystal based floating gate-type non-volatile memory is the very old charge trapping SONOS (silicon-oxide-nitride-oxide-silicon) or MONOS concept (using a metal gate electrode instead of silicon) [79, 80, 81]. An embedded silicon nitride (Si_3N_4) layer [see Fig. 1.2(b)] provides a considerable density of natural discrete traps, which allow a storage of both charge polarities in almost the same amount. The Si_3N_4 layer, which replaces the poly-Si floating gate in the classical Flash cell, is usually prepared by low-pressure chemical vapor deposition (LPCVD) [82]. The success of such devices was very limited suffering from a so called "erase saturation effect", where during Fowler-Nordheim erase the traps are refilled by electrons injected

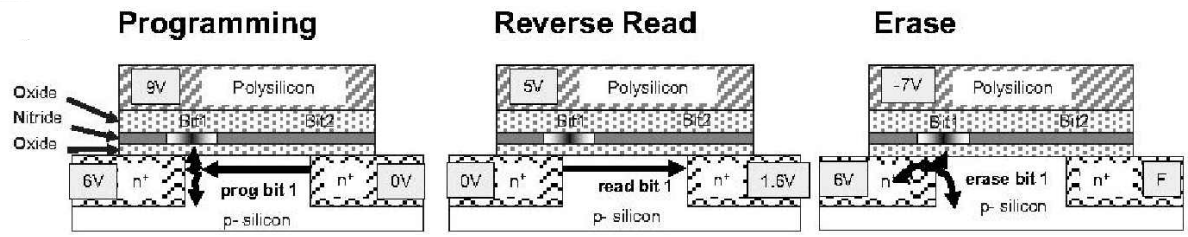


Figure 1.7: Concept of multibit charge trapping taken from Ref. [92].

from the gate [83]. Nevertheless, charge trapping memory cells have attracted special attention since in the late 1990s a 2-bit or multilevel charge storage was demonstrated utilizing channel hot electron and tunneling enhanced hot hole injection for programming and erase, respectively. In a so called nitrided-read-only-memory (NROM) cell [84, 85, 86] as shown in Fig. 1.7 the two bits are spatially separated and localized in the nitride layer of one transistor device, one close to the source and the other close to the drain contact. Such multibit devices are well established as, e.g., "Twin Flash^{TM}" (Qimonda) [87] or "MirrorBit®" (Spansion) [88] devices in the non-volatile memory microelectronic industry. Multilevel storage capability, which is supposed to be a key aspect in future memory devices, was also demonstrated for Si and metal NC containing memory devices [89, 78]. Thus, Si NC based memory devices are suitable for both NOR and NAND device architectures, where the programming is achieved by channel hot electron injection as in SONOS structures or by electron Fowler-Nordheim tunneling, respectively [15, 90]. There, the multibit capability can be reached by a different charge localization (SONOS trapping-like) or in a conventional floating gate operation due to a difference in the amount of stored charges (different value of threshold voltage shift). Combining the good cycling endurance and fast programming/erase ability of a nanocrystal based memory with a better data retention of SONOS devices, a hybrid Si nanocrystal/SONOS type memory transistor cell offers the opportunity of longer refresh times for, e.g., DRAM applications [91].

New gate insulator material systems including high-k materials (e.g., Al_2O_3) were introduced to solve the problem of erase saturation reducing the voltage drop over the topoxide layer. Simulations for NC based memory devices show that the programming and erase performance of such cells is significantly improved replacing the SiO_2 top oxide by a high-k dielectric [93]. Tantalum nitride or Pt are discussed as gate electrode materials to increase the barrier for electrons from the gate [94]. HfO_2/HfAlO/HfO_2 nanolaminates [95] prepared by atomic layer deposition (ALD) technique or TiN nanocrystals embedded in Al_2O_3 [96] can be also used as trapping layers in such devices replacing the sandwiched silicon nitride layer. Advanced device structures like FinFET [97] or 3D stacked [98] charge trapping memory cells have been recently developed with very promising results. Considering alternative future memory concepts the phase change memory seems to be the most competitive [92] as recently, a fully functional 512-Mbit phase-change random access memory (PCRAM) chip has been demonstrated [99]. An overview of recent and future memory concepts is given in the international technology roadmap for semicon-

ductors 2005 as shown in Fig. 1.8. The nanocrystal based memory devices are still an option for future non-volatile memories being fully compatible with other future charge trapping device concepts, i.e., the multibit storage, FinFET, 3D-structure etc. [92, 89]. After De Salvo *et al.* [15], the Si NC and the SONOS discrete-trap memory concept remain still promising candidates in future memory applications according to their costs per bit, their performance and reliability.

		Nano-floating Gate Memory [A]	Engineered Tunnel Barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	*Polymer* Memory	Molecular Memories
Storage Mechanism		Charge on floating gate	Charge on floating gate	Remanent polarization on a ferroelectric gate dielectric	Multiple mechanisms	Not known	Not known
Cell Elements		1T	1T	1T	1T1R or 1R	1T1R or 1R	1T1R or 1R
Device Types		1 Nanocrystal 2 Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-I-M 2 Solid Electrolyte 3 FE tunneling 4 FE Schottky diode 5 FE-I-FE	M-I-M (nc)-I-M	Bi-stable switch
Feature size F	Minimum required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	25 nm	10 nm [H]	22 nm [K]	5–10 nm [O]	5–10 nm	5–10 nm [AA]
	Demonstrated	90 nm [A]	180 nm [I]	~10 µm [L]	100 nm [P]	200 µm [W]	30 nm [AB]
Cell Area	Minimum required	$10F^2$	$10\ F^2$	$8F^2$	$10\ F^2$	$10\ F^2$	$10\ F^2$
	Best projected	$8–10F^2$	$8F^2$ [H]	$8F^2$	$8/5F^2$ [Q]	$8/5F^2$	$5F^2$
	Demonstrated	$16F^2$ [A]	Data not available	Data not available	Data not available	Data not available	Data not available
Read Time	Minimum required	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns
	Best projected	2.5 ns	2.5 ns	2.5 ns	<10 ns	<10 ns	<10 ns [AA]
	Demonstrated	20 ns [B]	20 ns [B]	20 ns [B]	2 ms [R]	~10 ns [X]	Data not available
W/E time	Minimum required	1 µs/10 ms	1 µs/10 ms	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	1 µs/10 ms	1 ns at 9V[H]	2.5 ns [B]	<20 ns [P]	Not known	<40 ns [AA]
	Demonstrated	W: 1–10 µs [C] E: 10–100 ms [D]	E: ~10 ms [I]	500 ns [L]	25 ns [P]	<10 ns [X]	~sec [AC]
Retention Time	Minimum required	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
	Best projected	>10 y	>10 y	>1y	>10 y	Not known	Not known
	Demonstrated	>200 hours [E]	>10 y [I]	30 days [M]	1 y [S]	6 month [Y]	2 months [AC]
Write Cycles	Minimum required	>1E5	>1E5	>1E5	>1E5	>1E5	>1E5
	Best projected	>1E5	>3E16	>3E16	>3E16	>3E16	>3E16
	Demonstrated	>1E4 [A]	5E4 [J]	1E12 [O]	1E5 [T]	>1E6 [X]	>2E3 [AD]
Write Operating Voltage (V)	Minimum required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	>3 V [F]	>3 V [F]	<0.9 V [K]	<0.5 V [U]	Not known	2 V [AE]
	Demonstrated	±6 [A]	6.5 [I]	±6 [O]	0.24 V [P]	~±2 [X]	~±1.5 V [AB]
Read Operating Voltage (V)	Min. required	2.5	2.5	2.5	2.5	2.5	2.5
	Best projected	0.7	0.7	0.7	<0.2 V [U]	0.7	0.3 [AA]
	Demonstrated	2.5 [B]	2.5 [B]	2.5 [B]	~0.2 V[P]	~1 [X]	0.5 [AB]
Write Energy (J/bit)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	5E-16 [G]	5E-16 [G]	2E-15 [N]	1E-15 [V]	Not known	2E-14 [AA]
	Demonstrated	2E-15 [G]	Data not available	Data not available	5E-14 [P]	1E-13 [Z]	Data not available
Comments		A natural evolution of the floating gate memory		Potential for non-destructive readout	Low read voltage presents a problem		
Research activity [AE]		123	12	74	39	25	68

Figure 1.8: Demostrated and projected parameters of emerging research memory devices as published in the ITRS 2005 [9].

2 Ion beam synthesis of nanocrystals in SiO_2 for nanodot memories

Ion implantation is a very important and widely used technique for the doping of silicon in the semiconductor industry (impurity concentration $N <$ solid solubility in silicon c). Impurity depth profiles are easily adjustable by ion energy (depth distribution) and fluence (doping level) - scalable and reproducible, whereas isotopically pure ion beams assure a low contamination of the wafer during processing. Its wide familiarity in the silicon technology makes it advantageous for future memory applications. As a versatile and very powerful technique, for research studies the ion implantation is used to synthesize nanoclusters/-crystals or nanocomposite materials ($N > c$) embedded in various host materials affecting the optical, magnetical, electrical or other properties of near-surface regions of the treated materials [100, 101, 102, 103].

This chapter addresses the principle of ion beam synthesis (IBS), especially the synthesis of semiconductor nanocrystals in thin gate oxides for the application in (non-) volatile memory devices. As a combination of ion implantation and subsequent annealing, IBS utilizes processes of self-organization in supersaturated and perturbed matrices via phase separation. Mainly tiny NC's (d_{nc} of 2 - 3 nm) are formed in a very high density ($N_{nc} \geq 1 \times 10^{12}\,\mathrm{cm}^{-2}$) in SiO_2 during annealing fulfilling one of the main requirements for future nanodot memory devices. Thin gate oxides ($\mathrm{d}_{ox} \leq 20$ nm) are required to realize devices with comparable or even lower programming voltages and times than of conventional floating-gate memories. In this chapter different IBS approaches are discussed with emphasis on the synthesis of NC's by low energy ion implantation - the main subject of this thesis. In a special case redistribution effects, i.e. combined processes of self-ordering and Ge diffusion, are utilized to obtain δ-like layers of Ge NC's in SiO_2 in vicinity to the Si substrate.

2.1 The principle of ion beam synthesis

From the technological point of view the ion beam synthesis is a combination of ion implantation at high fluences and subsequent annealing which is herein exemplified on Ge and Si ion implantation in thin gate oxides. The ion implantation of Ge or Si in SiO_2 leads usually to a supersaturation by impurity atoms inside the gate oxide due to a rather low solubility of these atoms in the oxide. Generally speaking, the depth distribution of the implanted impurities is nearly of Gaussian-type and is adjusted by the mass and energy (in keV) of the implanted ions. Their average penetration depth (projected range R_p) is determined by mass and energy, the mean NC size and density - at least to a

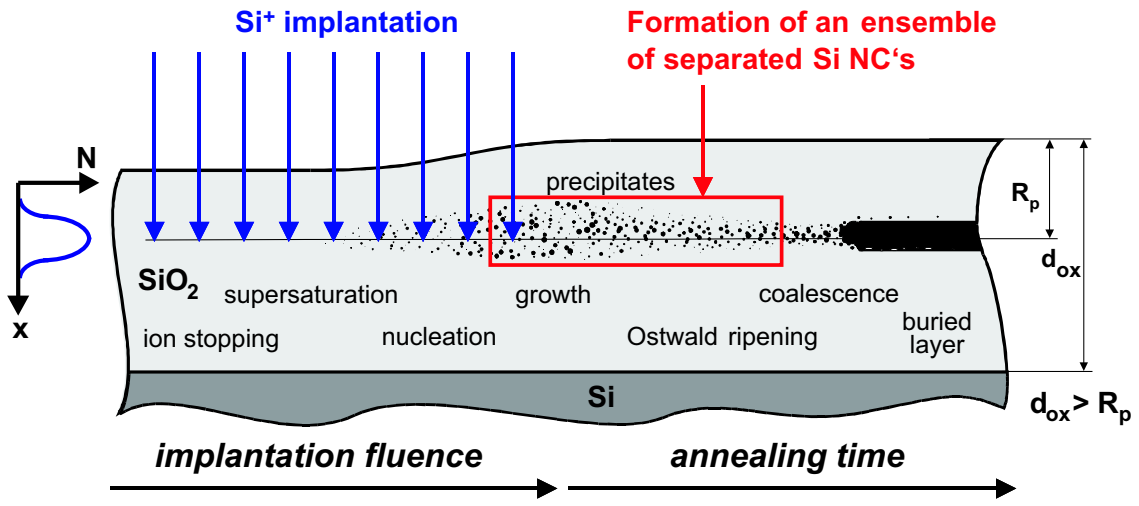


Figure 2.1: Scheme of ion beam synthesis of Si nanocrystals, for instance, deduced after Refs. [104, 105]. Even during ion implantation NC's nucleate inside the supersaturated region and grow in the following by subsequent annealing. Buried layers or wires can be formed for very high ion fluences by a process of coalescence.

certain extent [105] - by the implantation fluence (in ions/ cm^2). A subsequent thermal treatment is required to form the NC's by phase separation out of a supersaturated film and for damage annealing of the implanted oxide. The NC formation is described in terms of nucleation and growth of precipitates (Fig. 2.1). The NC mean size, density and spatial distribution changes during Ostwald ripening [106], whereas larger precipitates grow at the expense of smaller ones assuming an interaction between them by diffusion during the growth competition. The driving force of this process is the reduction of the total surface energy of the NC's and thus of the total free energy of the system by a mass transfer from dissolving small NC's toward larger ones. As a consequence, NC's of different size (radius R) have in thermal equilibrium different solute concentration of monomers in their surrounding media $c^{GT}(R)$, which is described by the Gibbs-Thomson relation [107, 104, 108].

$$c^{GT}(R) = c_\infty \, exp\left(\frac{R_c}{R}\right) \approx c_\infty \left(1 + \frac{R_c}{R}\right) \quad \text{with} \quad R_c = \frac{2\sigma V_m}{kT} \tag{2.1}$$

There, c_∞ is the solubility at a flat precipitate/matrix interface ($R \to \infty$) and R_c is the capillary length (σ, V_m, k, and T are the surface tension, the atomic volume, the Boltzmann constant and temperature, respectively). Thus, during annealing the final NC size distribution is governed by the Ostwald ripening process which disturbs a direct size (and size distribution) control varying only the ion implantation parameters. Lifshitz, Slyozov and Wagner (LSW) [109, 107] gave an analytical time-invariant solution of the NC size distribution in diffusion controlled systems ($t \to \infty$) assuming tiny nuclei embedded

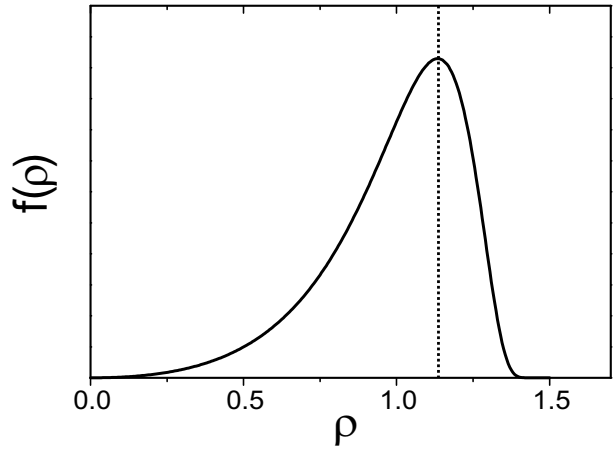


Figure 2.2: A typical normalized particle radius distribution after Lifshitz, Slyozov, and Wagner for diffusion controlled systems (maximum at $\rho = 1.135$) [107].

in a highly diluted solvent (volume fraction $\phi \to 0$) with an initially Gaussian-type size distribution (see Fig. 2.2).

$$f(\rho,t) = \frac{const.}{(1+t/\tau_D)^{4/3}} \rho^2 \left(\frac{3}{3+\rho}\right)^{7/3} \left(\frac{3/2}{(3/2)-\rho}\right)^{11/3} \exp\left(\frac{-\rho}{(3/2)-\rho}\right) \tag{2.2}$$

ρ is the a normalized NC radius with the mean particle radius $r^\star$, which is also a function of time.

$$\rho = r/r^\star \leq \frac{3}{2} \quad (f(\rho,t) = 0 \quad \text{for} \quad \rho > \frac{3}{2})$$

τ_D is a characteristic time constant of diffusion with diffusion constant D.

$$\tau_D = \frac{9[r^\star(t=0)]^3}{4c_\infty D V_m R_c}\,, \tag{2.3}$$

The LSW theory predicts that in the late stage of ripening the average NC radius evolves to the third potence with time t, i.e., the volume of tiny NC's ($\sim R^3$) dissolves proportional with time [110, 108].

$$\overline{R}^3(t) - \overline{R}^3(t=0) = K(\phi)\, t \tag{2.4}$$

The coarsening rate $K(\phi)$ is a monotonically increasing function of the volume fraction ϕ which does not change with time [110]. The NC density decreases with $1/t$ for $t \gg \tau_D$. These results are valid for diffusional problems, where the diffusion fields of the particles are not directly interacting (mean-field approximation) [108]. This mean-field approximation holds for Si excess volume fractions up to 10 at.% as shown in recent investigations for the ion beam synthesis of Si NC's in thick gate oxides (e.g., $d_{ox} = 800\,\text{nm}$) [111]. For higher volume fractions the multi-particle competitive growth problem can be solved by a

superposition of i diffusion fields of several (N) point-like sources (or sinks) of strengthes Q_i [110, 112, 108, 104, 113].

$$c(\mathbf{r}) \simeq c_u + \frac{1}{4\pi D}\sum_{i=1}^{N}\frac{Q_i}{|\mathbf{r}-\mathbf{r}_i|} \quad \text{with} \quad \lim_{|\mathbf{r}|\to\infty} c(\mathbf{r}) = c_u \tag{2.5}$$

Alternatively, kinetic Monte Carlo simulations were used to predict the NC size and density evolution [114]. In case of NC synthesis in very thin oxides (e.g., $d_{ox} \approx 10\,\text{nm}$) also a diffusional interaction with the close absorbing surface of the Si substrate has to be taken into account [114]. For a very high impurity atom supersaturation in the oxide (volume fractions higher than 20 - 30 at.%) coalescence of NC's occurs which finally may lead to a closed buried layer formation (see Fig. 2.1). This process is used, for example, to create a buried oxide layer in a Si wafer [silicon on isolator (SOI)] in the so called SIMOX technique (**s**eparation by the **im**plantation of **ox**ygen), where a high fluence oxygen ion implantation is carried out with subsequent high temperature annealing [115, 116].

2.2 Diffusion of Si and Ge in SiO_2

One of the key aspects of the nucleation and growth of Si, Ge or metal nanocrystals in SiO_2 during ion beam synthesis is the diffusion of impurities in the oxide. This topic is of fundamental interest for the preparation of NC's from Si rich oxides in general (whether prepared by deposition or implantation techniques) thinking of memory or optical applications. However, the detailed microscopic kinetics of diffusion within the oxide layer is still hardly understood, although SiO_2 is the most commonly used dielectric material in CMOS processing. Over the past two decades numerous experiments were carried out to enlighten the mechanism of Si diffusion in SiO_2, for instance. For this purpose different Si isotopes were used as tracers in stacked oxide layers, e.g., ^{30}Si atoms implanted in $^{28}SiO_2$ layers (see Tab. 2.1 and Fig. 2.3). In general, the diffusion is described as a thermally activated process using the well-known Arrhenius function

$$D \;=\; D_0\, exp\,(-E_A/kT) \tag{2.6}$$

with diffusion coefficient at infinite temperature D_0 (or $kT\,gg\,E_A$) and activation energy E_A (k is the Boltzmann constant and T the temperature). The focus lies on both the detection of the diffusing specie - which is not a trivial question - and its diffusion kinetics in SiO_2. Studying this way the self-diffusion of, e.g., Si and O gives also the perspective to understand the diffusion behavior of other (semiconductor) impurity atoms in SiO_2.

In the literature values for the diffusivity of Ge and Si atoms in SiO_2 vary over several orders of magnitude (see Fig. 2.3) which is most likely due to a significant influence of the different preparation and annealing conditions in the experiments. Also a dependence of the oxide layer thickness is reported as the Si self-diffusivity is clearly enhanced in thinner oxides, where the Si/SiO_2 interface is located closer to the region of Si excess [117, 118]. Considering a typical value for the diffusion coefficient of Si, Ge or O atoms in SiO_2, e.g., $D \leq 10^{-17}\,\text{cm}^2/\text{s}$ at $T \leq 1050°\text{C}$ (see Fig. 2.3 and Tab. 2.1), the corresponding diffusion

Table 2.1: Coefficients for the diffusion of Si and Ge atoms in SiO_2. Exemplarily, the diffusivity at $T = 1050°C$ is specified varying in the case of Si diffusion over at least four orders of magnitude. The labelled references refer to the data in Fig. 2.3.

element	D_0 [cm^2/s]	E_A [eV]	$D(1050°C)$ [cm^2/s]	Ref.	topic
Si	544.7	6.16	1.9×10^{-21}	[121]^a	not specified
	328	6.0	4.6×10^{-21}	[122]^b	$^{30}SiO_2$ on $^{28}SiO_2$
	1.2×10^{-9}	1.9	6.9×10^{-17}	[120]^c	Si NC growth in SiO_2
	1.378	4.74±0.25	1.2×10^{-18}	[123]^d	$^{30}Si^+$ implant in $^{28}SiO_2$
	33.2	5.34	1.5×10^{-19}	[124]^e	SiO_2 on $^{28}SiO_2$
		0.26	$>4\times10^{-13}$	[125, 126]	sputtered SiO_2
Ge	537	5.38	1.7×10^{-18}	[121]^a	not specified
	7250	5.69	1.5×10^{-18}	[127]^f	Ge^+ implant in SiO_2
	8.9×10^{-3}	3.9	1.2×10^{-17}	[128]^g	Ge doped SiO_2 on SiO_2
O	2.6	4.7	3.2×10^{-18}	[129]^h	$Si^{16}O_2$ on $Si^{18}O_2$

length $L_D = \sqrt{Dt}$ yields only some angstroms (< 4 Å) and below for a thermal annealing of 120 s. Such low values clearly contradict the observed formation of Si or Ge NC's in SiO_2 for thermal treatments at moderate temperatures and times ($T \ll 1100°C$ for less than 120 s) and also to the significant redistribution of Ge in SiO_2 as reported in chapter 5 for $T \leq 950°C$ annealing. 3D-kinetic Monte Carlo simulations reveal that under these circumstances ($T = 1050°C$) the formation of Si NC's in thin oxides would take hours, not seconds as found by recent experiments [119]. However, a slightly higher diffusion coefficient ($D = 6.9 \times 10^{-17}$, $T = 1050°C$) is deduced studying the Si NC growth [120].

So far, the diffusion of Si in SiO_2 has been mainly discussed in terms of Si self-diffusion considering Si interstitials as the diffusing specie in the oxide [123, 124, 120, 122]. But, theoretical calculations reveal that models based on the formation and diffusion of isolated point defects (interstitials and vacancies in the classical sense) are likely misleading [130]. As a consequence, a mechanism of diffusion different from simple Si interstitial motion in SiO_2 should be considered. SiO molecules, which are generated at the Si/SiO_2 interface and emitted from there into the SiO_2 network during thermal treatment, are supposed to enhance the Si self-diffusivity in SiO_2 [131]. As shown by Uematsu *et al.* [118] this approach is suitable to explain the oxide thickness dependence on the diffusivity found by Fukatsu *et al.* [117]. But, the idea of SiO molecules squeezing through the oxide at elevated temperature without any interactions with the covalent SiO_2 network seems to be more than questionable [132]. However, as shown in Tab. 2.1 the energy of activation for the motion of Ge or the self-diffusion of Si or O in SiO_2 is conspicuously rather similar for all (about 5.4 ± 0.7 eV), despite the different experimental conditions in the diffusion experiments. Thus, a common diffusion mechanism or specie should be considered.

In this thesis (chapters 5 and 9) an oxygen vacancy mediated diffusion mechanism in

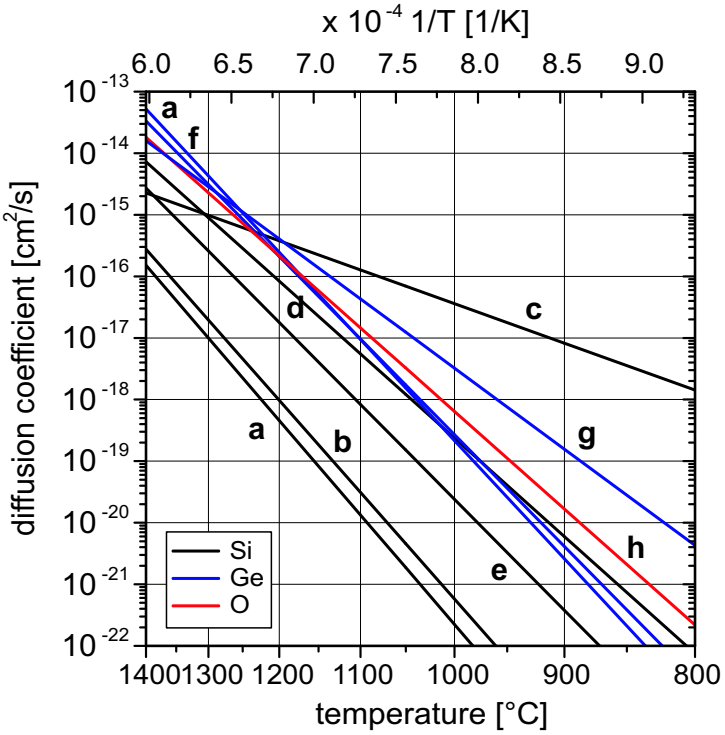


Figure 2.3: Diffusion coefficients for Si, Ge or O in SiO_2 as a function of annealing temperature calculated from data as summarized in Tab. 2.1.

SiO_2 is proposed. The oxygen vacancy is the most common defect in SiO_2 [133]. An oxygen atom displaced from the SiO_2 network leaves two dangling Si bonds behind as the so-called bridging (Si-Si) or non-bridging (Si· ·Si) oxygen-deficiency centers. It is known from *ab-initio* calculations that such defects have a very low energy of formation, especially at Si/SiO_2 interfaces [134, 135]; the energy of migration in SiO_2 is just 1.7 - 1.9 eV [136]. Migrating oxygen-vacancies induced long-range distortions in the SiO_2 network [133]. Thus, the Si diffusion in SiO_2 can be described as an effective process of multiple matrix perturbing and mixing events. In chapter 5 the enhanced diffusion of Ge in SiO_2 is explained in a similar way with the same diffusing specie being involved. Here, the Ge impurity atom gains a higher diffusivity sticking to an energetically favored position close to the highly mobile oxygen vacancies. This process is similar to the well-known transient enhanced diffusion of boron in Si bulk material [137], where the impurity atom diffusion is mediated by Si self-interstitials and not by oxygen vacancies as in SiO_2.

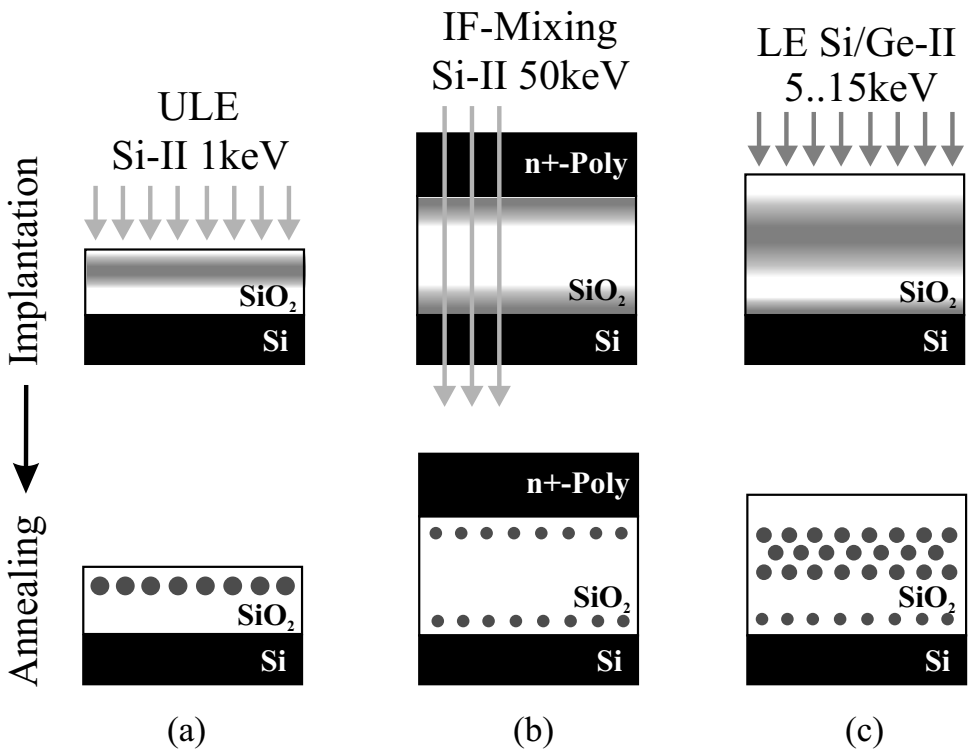


Figure 2.4: Main concepts of NC ion beam synthesis for nanodot memories. The ion implantation (II) is performed with different ion energies in or through 8, 15 and 20 - 30 nm thin oxide layers (typical sizes) in (a) - (c), respectively.

2.3 Different approaches for ion beam synthesis of NC's in thin SiO_2 layers

Figure 2.4 shows the three main routes of NC ion beam synthesis in thin oxide layers ($d_{ox} \leq 30$ nm) aiming at memory device applications. The choice of different ion energies and oxide thicknesses results in different NC distributions after annealing. (i) A very shallow Si ion profile is realized close to the oxide surface after annealing as shown in Fig. 2.4(a) using Si^+ ultra-low-energy (ULE)-implantation ($E \approx 1$ keV) at fluences of $D \geq 1 \times 10^{16}\,\mathrm{cm}^{-2}$ in $d_{ox} \leq 10\,\mathrm{nm}$ thin SiO_2 layers which yields a very high peak Si excess of ≥ 33 at.% in the oxide [114]. (ii) A completely different approach is pursued irradiating a poly-Si(Gate) | SiO_2 | Si(bulk) layer stack [Fig. 2.4(b)]. Collisional cascades of displaced atoms lead to a mixing of both formerly sharp Si/SiO_2 interfaces. During subsequent annealing and interface reconstruction a rather symmetric arrangement of Si NC's forms embedded in SiO_2 in vicinity to both electrodes, the poly-Si gate and Si bulk layer. (iii) By low-energy (LE)-implantation [Fig. 2.4(c)] both components - primary implanted Si ions and backward mixed Si atoms - contribute to the resulting NC distribution. A comparison of Si and Ge ion implantation reveals that in the latter case additionally a redistribution of Ge during annealing has to be taken into account. Each of these

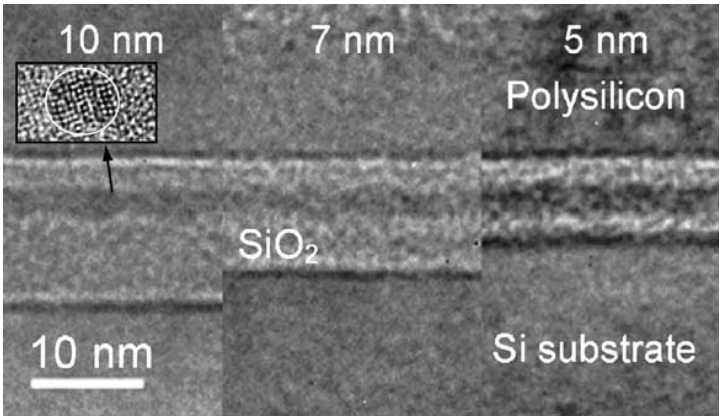


Figure 2.5: High resolution cross section TEM images under defocused bright field conditions according to identical ULE ion implantation and annealing parameters performed in 10, 7 and 5 nm thin oxides [138].

concepts is discussed in the following exemplarily, whereas this thesis focuses on the low energy Si^+ or Ge^+ implantation shown in Fig. 2.4(c).

Ultra-low-energy (ULE) ion implantation

The ULE ion beam synthesis is carried out in thin gate oxides (5 - 10 nm) as shown in Fig. 2.5 with a Si ion energy of 1 keV at high Si^+ fluences ($1\times10^{16}\,cm^{-2}$) [138, 139, 140]. As a consequence, the Si excess in SiO_2 yields about 35 at.% at the profile maximum [140] resulting in a significant swelling of the oxide layer. High fluences are mandatory due to a high sensitivity of the near-surface implanted Si impurities to oxidants (mainly H_2O) from handling, cleaning and annealing ambience (see also chapter 2.7). The introduced oxygen reduces the amount of Si available for the NC formation during subsequent annealing causing a parasitic oxide growth ($Si + O_2 \rightarrow SiO_2$ or $Si + 2H_2O \rightarrow SiO_2 + 2H_2$). Kinetic lattice Monte Carlo (KLMC) simulations reveal that for such a high Si excess the process of NC formation has to be discussed in terms of "spinodal decomposition" and percolation [114]. Indeed, the transmission electron microscopy (TEM) images in Fig. 2.5 show crystalline areas embedded in a closed Si layer [138, 141]. This indicates the formation of in-plane structurally and/or electrically connected Si NC's rather than of isolated and well separated ones. The annealing is typically carried out at temperatures of $T \geq 950°C$ for at least 30 min in N_2 or Ar atmosphere. An additional content of 1.5% O_2 in the annealing gas has a beneficial effect on the data retention of such devices (long-term extrapolation indicates a 10-year retention with a memory window of about 0.4 V) [138]. A memory window of ~ 2 V is achieved (difference in the threshold voltage between the programmed and erase state) with write/erase pulses of ± 9 V for durations of ≥ 10 ms. Neither degradation nor drift in memory window was detected after 10^6 write/erase cycles. Although the Si NC containing layer is positioned closer to the gate than to the Si bulk electrode - as clearly shown in Fig. 2.5 for ULE IBS in a 7 and 10 nm SiO_2 layer - it is reported that the main charge exchange of the NC layer occurs

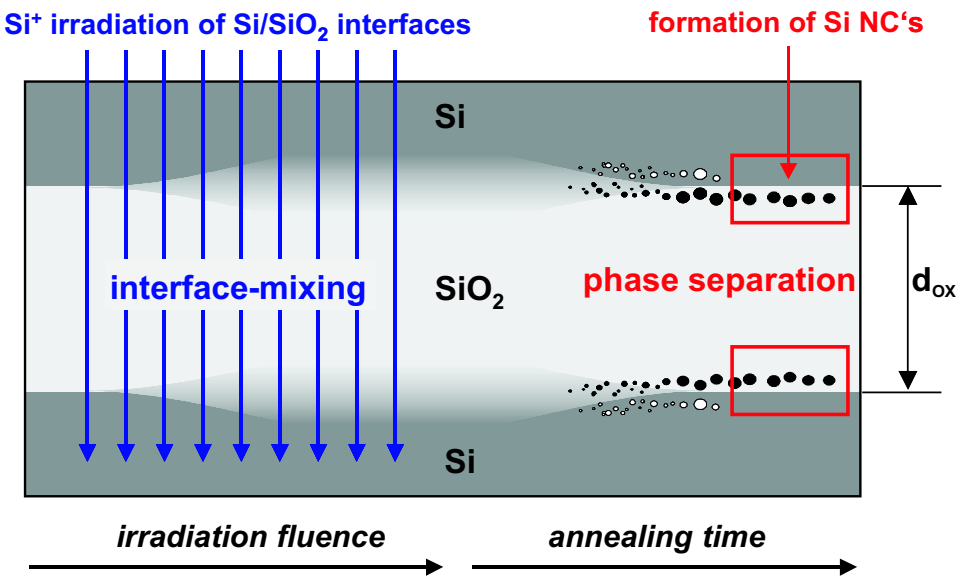


Figure 2.6: Two self-aligned Si NC δ-layers form in SiO_2 by irradiation of both Si/SiO_2 interfaces of a poly-Si/SiO_2/Si-substrate stack and subsequent annealing (scheme taken from Ref. [145]).

with the Si substrate and not with the gate [138, 139]. Thus, the mechanism of charge transfer through the oxide related to the Si substrate is supposed to be trap-assisted. An attempt to reduce the tunneling distance between the Si NC layer and the Si substrate below 5 nm increasing the implantation energy failed [140]. A direct tunneling distance of about 2 nm can only be achieved by the implantation of Si ions in thinner gate oxides (e.g., in 5 nm as in Fig. 2.5). The deposition of an additional control oxide (20 - 30 nm) onto the thin ULE implanted SiO_2 layer ensures that the Si NC layer is located closer to the Si substrate than to the gate [142, 143, 144].

NC formation by interface irradiation

Here, the supersaturation of Si in the oxide is not directly related to the implanted Si species. The Si excess near the Si/SiO_2 interfaces is achieved just by ion irradiation through a stack as presented in Fig. 2.4(b) and 2.6, in principle more or less independent on the type of ion. The concept of NC formation by irradiation is protected by patents for device-relevant applications [147]. A 50 nm n^+-poly-Si gate covers 15 nm SiO_2 grown on p-Si [148, 149, 145]. This stack is irradiated by 50 keV, 1×10^{16} Si ions/ cm^2, for instance. The majority of implanted Si ions is positioned deeply in the Si bulk, thus a direct introduction of those atoms into the SiO_2 layer and therefore a contribution to the NC formation is negligible. During the ion irradiation Si and O matrix atoms are displaced and mixed by collision cascades with the consequence that both formerly sharp Si/SiO_2 interfaces get smeared out. Si atoms from the Si substrate (and the poly-Si

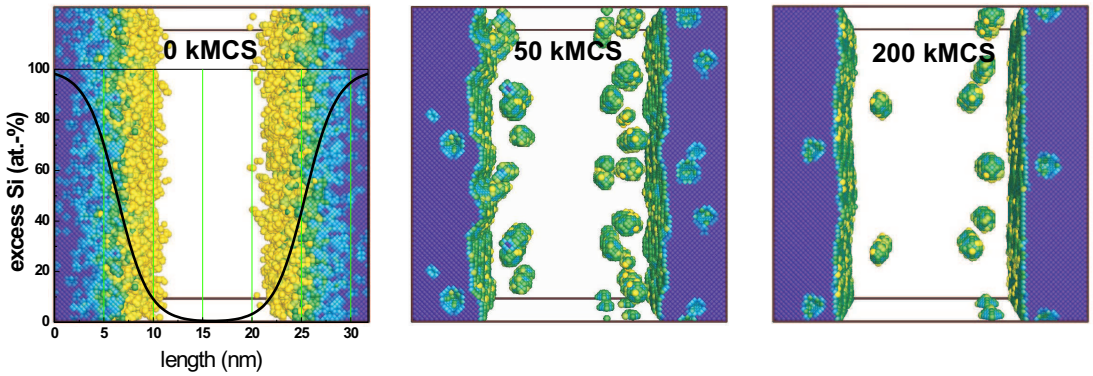


Figure 2.7: 3D KLMC simulation of an irradiated stack as presented in Fig. 2.4(b). The color-scales reflect the number of diatomic Si-Si bonds. After 50000 MC steps Si NC's and SiO_2 clusters are formed in the SiO_2 and in the Si bulk, respectively. With proceeding simulation/annealing time the Si/SiO_2 interface gets smoother and the NC's dissolve until an equilibrium of totally separated regions is reached. The KLMC simulation was performed by K.-H. Heinig, Forschungszentrum Rossendorf 2003 (see also Refs. [104, 114, 146]).

gate) come to rest inside the oxide and oxygen atoms from SiO_2 are displaced into the Si substrate (and the poly-Si gate). The expected Si excess in the sandwiched oxide layer for the as-implanted state is shown in the inset of Fig. 2.7(a). During subsequent annealing ($T \geq 950°C$) the instable mixture of Si and SiO_2 starts to separate. The process of interface restoration and NC formation is confirmed by KLMC simulations as shown in Fig. 2.7. During re-formation of the interfaces some Si atoms, which are displaced deeper into the oxide, stay within the SiO_2, form precipitates and grow to NC's (see also Fig. 2.6). The same happens to displaced O atoms within the Si bulks forming SiO_2-clusters in the gate and substrate. The number of Monte Carlo (MC) steps corresponds to annealing temperature and time. Aspiring towards equilibrium conditions the Si and SiO_2 clusters disappear with on-going annealing time, but due to the higher mobility of O in Si than Si in SiO_2 the Si NC are far more stable. The process of dissolution and growth can be described by means of Gibbs-Thompson relation and Ostwald ripening [105].

As indicated in the Figs. 2.6 and 2.7(c), after annealing two layers of tiny NC's (size $\approx$1 - 3 nm) form almost symmetrically in vicinity to each of the Si/SiO_2 interfaces. They are self-aligned and separated to the Si-gate and substrate electrode by SiO_2 zones of 1 - 3 nm thickness denuded of Si. The distance depends on the degree of interface-mixing (i.e. the implantation fluence), annealing temperature, and time. Energy-filtered (EF-)TEM and decoration experiments prove the existence of the Si NC's, as the direct detection by fringes in conventional high resolution (HR) cross section TEM failed [149, 150]. This concept has the outstanding advantage that the irradiated SiO_2 region is covered by a poly-Si gate; thus, the cleaning and annealing ambience does not affect the most sensitive gate oxide region during the NC synthesis processing. Electri-

Table 2.2: Parameter for low energy Si, Ge, and Au ion implantation for memory applications in gate oxides with different thickness d_{ox}. Reported data of ion energies, fluences and annealing conditions are listed in chronological order in comparison to those used in the present thesis.

ion	energy [keV]	fluence [cm^{-2}]	d_{ox} [nm]	annealing	references
Si	10 - 25	0.4 - 2×10^{16}	20 - 35	1000°C, 1 h, N_2	Kalnitsky *et al.* [151, 152]
	25	3×10^{16}	50	900°C, 30 min, N_2	Hori *et al.* [153]
	10	3×10^{15}	21.6	900°C, 20 min	Hao *et al.* [154]
	20 - 50	0.1 - 3×10^{16}	50	900°C, 30 min, N_2	Ohzone *et al.* [155, 156]
	5	5×10^{15}	20	950°C, 30 min, N_2	Hanafi *et al.* [21]
	6 - 12	0.5 - 1×10^{16}	20 - 30	1050°C, 30 - 60 s, N_2	v. Borany *et al.* [157, 158]
	15	2×10^{16}	20	1100°C	Porti *et al.* [159]
	6	0.7 / 2.0×10^{16}	20	1050°C, 30 - 120 s, Ar	this thesis
Ge	10 - 20	0.07 - 1×10^{16}	5 - 20	950°C, 30 min, N_2	Hanafi *et al.* [21]
	12 - 20	3.5 - 7×10^{15}	20 - 30	1050°C, 30 - 60 s, N_2	v. Borany *et al.* [157, 160]
	13 - 17	1 - 2×10^{16}	28 - 30	700 - 1050°C, 30 min, N_2	Duguay *et al.* [35, 161]
	15	0.5 - 2.5×10^{16}	30 - 50	800 - 1050°C, 10 min, Ar	Kim *et al.* [162]
	12	0.5 / 1.5×10^{16}	20	950 - 1050°C, 30 s, Ar	this thesis [163, 75]
Au	30	4×10^{15}	30	1000°C, 10 - 60 min, N_2	Beyer *et al.* [164]

cal investigations of such samples annealed at 1050°C for 30 s in N_2 show clear memory behavior [145, 148]. Write/erase-pulses of 10 ms at voltages of ± 6 V reach programming windows of about 0.6 V with a data retention of hours at 85°C. A trade-off between the degree of mixing and NC size, density and their distance to the Si bulk limits the application for memory devices. A stronger perturbation for larger injection distances needs a higher temperature budget for reconstruction. As a consequence larger NC's ripen with significantly reduced NC density.

2.4 Low energy Ge and Si ion implantation, Ge redistribution and loss

The third [Fig. 2.4(c)] and main concept in the present thesis deals with low energy (LE) ion implantation (II). As summarized in Tab. 2.2 the LE ion beam synthesis of NC's is usually performed with 5 - 20 keV Si or Ge ions at fluences of 0.5 - 2×10^{16} cm^{-2} in 20 - 30 nm thin gate oxides. The impurity excess in SiO_2 reaches about 5 - 20 at.% at the maximum of the Gaussian shaped ion profile. During annealing for several seconds or minutes at 900 - 1100°C the NC's form mainly close to the oxide center, Ge NC's at lower temperatures ($T > 750$ - 900°C [165]) than Si NC's ($T > 1000$°C [166, 167]). The

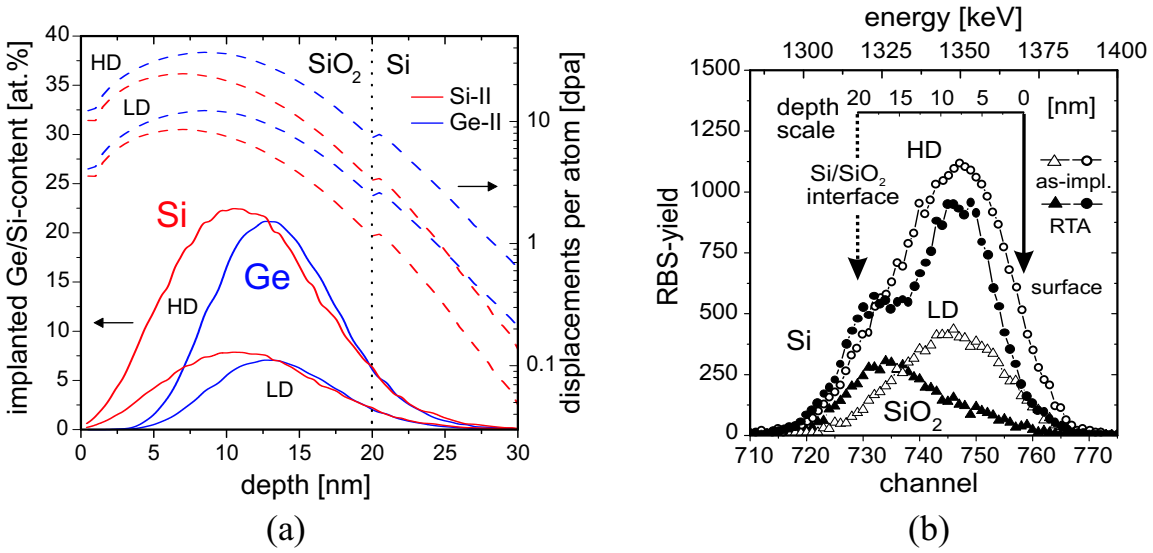
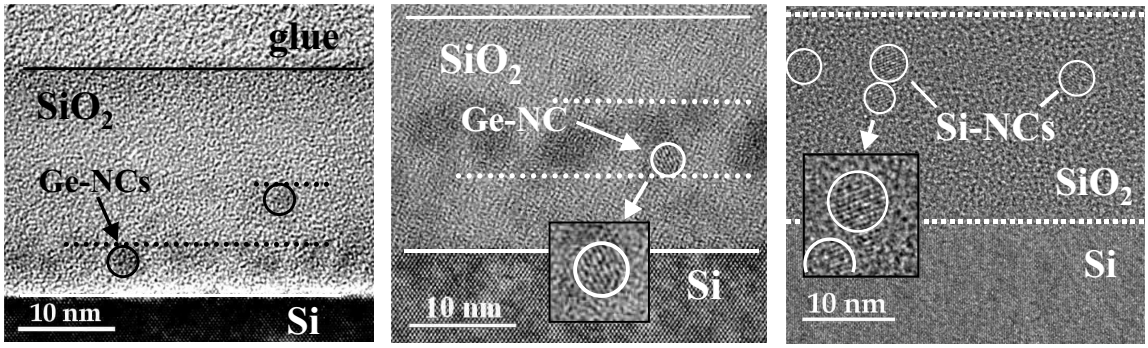


Figure 2.8: (a) Calculated profiles for Si (red) and Ge (blue) ion implantation into 20 nm thin SiO_2 layers (left ordinate) using the SRIM 2000 code [175, 176]. The corresponding number of displacements is indicated by broken lines (right ordinate). The profiles are obtained for two fluences each, a low (LD) and a threefold higher one (HD), related to the ion energies and fluences listed in Tab. 2.2). (b) A significant Ge redistribution and loss was obtained by Rutherford backscattering spectrometry (RBS) after rapid temperature annealing (RTA) at 950°C for 30 s in Ar. The presented data were previously published by Springer-Verlag Berlin, 2005 [177] including also the corresponding images shown in Fig. 2.9.

LE Si^+ or Ge^+ implantation provides broad impurity profiles in the oxide (see Fig. 2.8). Taking into account the diffusion of these atoms in SiO_2 during the subsequent thermal treatment, an enrichment of the Si substrate with the implanted Ge is inherent for this type of ion beam NC synthesis. Thus, the choice of the incident ion element is restricted to Si and Ge as the latter is completely miscible with Si in the substrate. Moreover, the Ge incorporated in SiO_2 forms nanocrystals (similar to Si) or oxidizes to GeO_2 in a structure matching to the silicon oxide network. In contrary, a contamination of the substrate with fast diffusing metal impurities like, e.g., Cu, Fe or Au is clearly not acceptable in modern microelectronic memory device processing [164]. Indeed, Ge is discussed to cause a high density of charge trapping states at the Si/SiO_2 interface [168], but Ge incorporated in Si can also have a very beneficial function. Strained Si_{1-x}/Ge_x layers yield a significantly enhanced hole mobility in a MOSFET transistor channel in comparison to equivalent Si devices [169, 170]. Such layers can be also prepared by Ge ion implantation and subsequent solid phase epitaxy during annealing [171, 172, 173, 174].

In the early 1990s Kalnitsky *et al.* [151, 152] noticed a considerable charging effect after annealing of Si implanted 20 - 35 nm thin oxide layers (data see Tab. 2.2). In the following years several investigations concerning possible memory applications were carried out by Hori and Ohzone *et al.* [153, 155, 156]. The charging was referred to



(a) Ge NC-IBS (LD) (b) Ge NC-IBS (HD) (c) Si NC-IBS (HD)

Figure 2.9: Cross section bright field TEM micrographs in high resolution according to the Si and Ge low energy ion implantation profiles shown in Fig. 2.8(a). The annealing was carried out at 950 (Ge) or 1050°C (Si) for 30 s in Ar. (a) A redistribution of Ge yields the formation of a δ-layer of Ge NC's in vicinity to the Si/SiO_2 interface. (b, c) Higher fluence ion beam synthesis (HD) reveals the Ge or Si NC's mainly close to the oxide center corresponding to R_p. For the Si^+, LD implantation case NC's were not detected.

oxide traps, however generated by damage defects induced by the ion implantation or by the incorporated Si atoms. However, Hanafi *et al.* [21] proved that the memory effect is related to the existence of NC's in the gate oxide independent of the fabrication method, ion beam synthesis or chemical vapor deposition. Later on, in a cooperation of Zentrum Mikroelektronik Dresden (ZMD) with Forschungszentrum Dresden - Rossendorf (FZD) metal-oxide-semiconductor (MOS) capacitors and single MOS- field effect transistors (MOSFETs) were prepared with embedded Si or Ge NC's in thin gate oxides utilizing the low energy Si and Ge ion implantation [157, 36, 160, 158]. Very promising charge storage characteristics were reported for these devices including charge retention measurements on wafers stored at 150°C and 250°C to achieve comparable data to concurring memory concepts. Finally in 2001, for Si^+ implanted gate oxides a first functional 256k-non-volatile static random access memory (nvSRAM) was demonstrated [157, 158]. The Ge implanted oxides reveal a larger programming window than the Si implanted ones (10 ms programming pulses of 10 - 15 V), but also a weaker data retention (in the range of minutes for Ge and hours or days for Si) [157, 36]. A good endurance behavior was obtained without any device degradation after 10^5 write/erase cycles for both types. But, the location of the stored charge (in the NC's, at traps at or in the NC's or at oxide traps) as well as the current conduction mechanism through the oxide were still the very fundamental and open questions.

The present thesis regards the Si and Ge implantation in 20 nm thin gate oxides as shown in Fig. 2.8(a). The studies focus on changes in the oxide composition induced by the ion implantation and the subsequent annealing as well as on the electrical properties of the Si and Ge NC containing gate oxides. The annealing causes a significant redistribution and loss of the introduced Ge [Fig. 2.8(b)] which yields clear differences in the final NC distributions in SiO_2 depending on the implanted fluence [see the cross section

transmission electron microscopy (TEM) images in Fig. 2.9(a, b)]. Preliminary investigations of the memory properties of Ge NC containing MOS capacitor devices promise flatband voltage shifts of about 1 V even with programming pulses of 8 V applied for 1 μs [Ge NC-IBS, LD; Fig. 2.9(a)] [177]. Using 100 ms $\pm$ 8 V write/erase pulses, programming windows of about 8 V are achieved, which unfortunately decay in the range of seconds waiting time. For the Si implanted oxides no comparable redistribution effect was obtained. There, a programming window of 1.5 V is realized under the same conditions as for Ge which saturates at about 2 V for longer and/or higher programming pulses. A window of at least 0.5 V remains after hours or days waiting time.

Utilizing the Ge redistribution effect to prepare Ge NC memory devices

The redistribution of Ge toward a multimodal impurity distribution during annealing with a considerable accumulation of Ge in vicinity to the Si/SiO_2 interface was first recognized for Ge ion implantation in thick ($d_{ox} \geq 100$ nm) SiO_2 layers [168, 178, 179, 180, 181, 182]. As succeeded in Fig. 2.9(a) the redistribution effect can be utilized to fabricate a δ-like layer of Ge NC's in thin oxides (20 - 30 nm) very close to the Si/SiO_2 interface [35, 183, 184]. This structure satisfies the demands of future nanodot memory devices (see chapter 1.3 and Fig. 1.8) with the perspective of low programming voltages and/or times [160, 163, 177]. As shown in Fig. 2.8(a) with the Ge^+ implantation a fraction of ions reaches the Si substrate. As a consequence, collisional mixing at the Si/SiO_2 interface occurs which results additionally in an Si excess in the oxide, similar to that discussed previously for the NC formation by interface irradiation. Experiments show [183] that a damage rate of about 1 displacement per atom at the Si/SiO_2 interface is needed to build such a near-interface NC band. During annealing phase separation occurs and small Si precipitates form in SiO_2 close to the Si substrate, similar to Fig. 2.6 and 2.7 but for a single interface [105, 183]. At the same time, the thermal treatment yields that Ge atoms diffuse through the oxide toward the Si substrate [see the LD case in Fig. 2.8(b)], get trapped at the emerging Si precipitates, and nucleate there to grow to Ge (or Ge_xSi_{1-x}) NC's. As discussed to Fig. 2.7 the Si NC disappear with ongoing annealing time, but in this case these sites get stabilized by the accumulating Ge. Besides the in-diffusion of Ge, the redistribution is usually also associated with a Ge out-diffusion which causes inherently a partial loss of the implanted Ge amount [see Fig. 2.8(b)]. Additionally to the interface mixing, an amorphization of the Si substrate within the first 5 - 10 nm has to be taken into account. But, during annealing solid-phase epitaxy yields a re-crystallization of this region. TEM and large area x-ray reflection measurements (using synchrotron radiation) reveal a complete recovery of the Si substrate, and a very smooth Si/SiO_2 interface re-forms with a rms-roughness of about 0.4 nm [157].

The phenomenon of Ge redistribution and loss

For thick SiO_2 films ($d_{ox} > 100$ nm) the influence of implantation and annealing conditions on the Ge redistribution has been studied by numerous investigations [168, 178, 179, 181, 182, 184, 185, 186]. However, the detailed mechanism of this behavior remains

under discussion. It is widely accepted that both, redistribution and loss are strongly influenced by moisture contaminants (H_2O, OH) which penetrate the damaged oxide after ion implantation (for details see chapter 2.7) [187]. These species originate either from air humidity and wet cleaning chemicals ("intrinsic source") or from the residual moisture in the "inert" Ar or N_2 annealing ambience ("extrinsic source"). The "intrinsic" are inevitable sources within the ion beam synthesis processing. During annealing the excess oxygen and hydrogen may react with Ge leading to the formation of amorphous GeO_2 and mobile (volatile) compounds like GeH_4 or GeO. In detail, the effect of Ge oxidation during annealing was studied by Heinig *et al.* [179] and Borodin *et al.* [186] for 500 nm SiO_2 films. Their kinetic 3D lattice Monte-Carlo (KLMC) simulations consider the diffusion of two kinds of interacting impurities - dissolved Ge monomers and an oxidizing component (e.g., O_2 or OH). The simulated Ge redistribution and the formation of near-surface GeO_2 are in good agreement with the experimental results obtained by x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) [185]. But, as the GeO_2 is spatially fixed, a considerable Ge loss of $\sim 50\%$ as found by Markwitz *et al.* [178, 188] can not be explained by this model. This loss occurred after a furnace annealing of Ge implanted SiO_2 films at $T = 1100°C$ in $Ar + 7\% H_2$. It was attributed to volatile GeH_4 or GeO but no experimental evidence has been reported. Recently, Marstein *et al.* detected also voids in thick oxides after Ge implantation and long-term annealing [189]. Such impact and chemical reactions of Ge with oxidizing (and reducing) species - namely the Ge redistribution and the Ge loss - should be much more pronounced in thin gate oxides, where the implanted Ge is located very close to the surface. But for this device relevant case, no detailed study has been carried out so far. Thus, as one of the main parts of the present thesis, this topic is extensively discussed in chapter 5 (see also chapter 2.2).

2.5 Ion depth profile calculation using TRIDYN

Penetrating the target matter, an implanted (usually singly positively charged) ion looses its energy with substrate depth x due to interactions with the target atoms. The stopping powers $\mathrm{d}E/\mathrm{d}x$ in the materials are determined by the Coulomb interactions with positively charged nuclei [nuclear stopping $(\mathrm{d}E/\mathrm{d}x)_{nuclear}$] and with the negatively charged electron shell of the target atoms [electronic stopping $(\mathrm{d}E/\mathrm{d}x)_{electr.}$]. The total stopping cross section in matter S_{tot} is the sum of these stopping powers S_n, S_e and the density of atoms N [at./cm^3] in the target.

$$S_{tot} = S_k(E) + S_e(E) = -\frac{1}{N}\left\{\left(\frac{dE}{dx}\right)_{nuclear} + \left(\frac{dE}{dx}\right)_{electr.}\right\} \tag{2.7}$$

The elastic interactions with the nuclei Coulomb potentials is responsible for target atom displacements and the electronic energy loss causes bond breaking and phonon energy deposition. As shown in Fig. 2.10 in SiO_2 the nuclear stopping power considerably exceeds the electronic energy loss in the low energy range (< 20 keV) of Ge and Si ion implantation mainly used in this thesis.

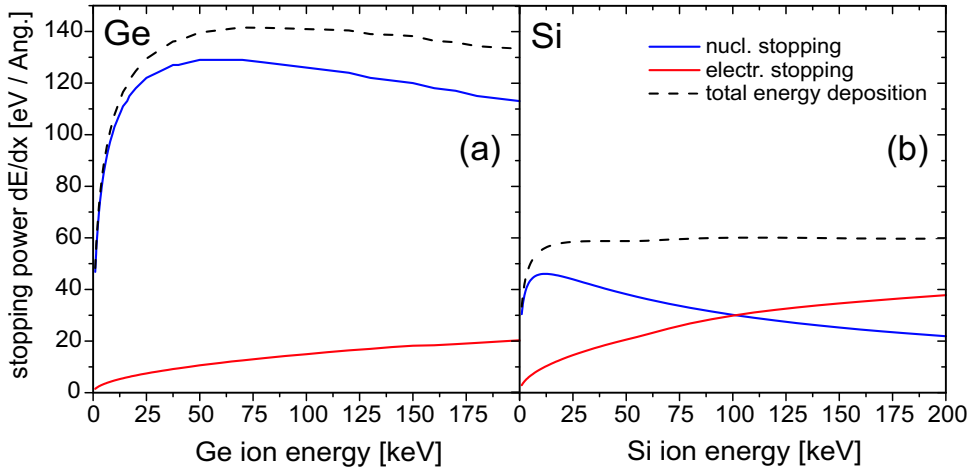


Figure 2.10: Nuclear and electronic stopping powers related to Ge (a) and Si (b) ion implantation into SiO_2 ($\rho = 2.27\,g/cm^3$) for ion energies $E \leq 200$ keV.

In principle the initial impurity atom depth distribution $N(x)$ in the target material after ion implantation has approximately a Gaussian-like profile shape

$$N(x) = \frac{D}{\sqrt{2\pi}\Delta R_p} exp\left[-\frac{(x-R_p)^2}{2\Delta {R_p}^2}\right] \tag{2.8}$$

with an average projected range R_p in oxide depth x and its straggling ΔR_p. A "Pearson-type-IV" distribution takes additionally a skewness and kurtosis of the profile into account [190, 191]. For more reliable information about the actual ion distribution in the target enclosing information about the introduced structural damage in the media, the SRIM code should be used [192]. Typical Ge ion implantation cascades are shown in Fig. 2.11. All kinetic phenomena associated with the energy loss of the incident ions in the target are included, namely the target atom displacements, the sputtering, the ionization effects, and the energy transfer to phonons. The calculation is based on Monte Carlo range algorithms developed by J. P. Biersack *et al.* [176]. A full description of the SRIM program and also a detailed explanation of the physics of the ion interactions in solids is given in Ref. [175]. In this thesis, the ion implantation depth profiles are calculated by means of a dynamic binary-collision computer simulation code called TRIDYN [193]. There, the commonly used SRIM program is extended to dynamic changes in the substrate thickness and composition due to swelling and surface erosion effects which have to be taken into account for ion implantations at high fluences. This code computes depth profiles of all atomic species in the target as a function of the incident fluence including sputtering yields, total areal densities, surface concentrations and re-emitted ion amounts.

TRIDYN input parameter

For the TRIDYN ion profile calculation parameters of the incident ion beam (ion energy, element and fluence), the target structure (composition, atomic density for each compo-

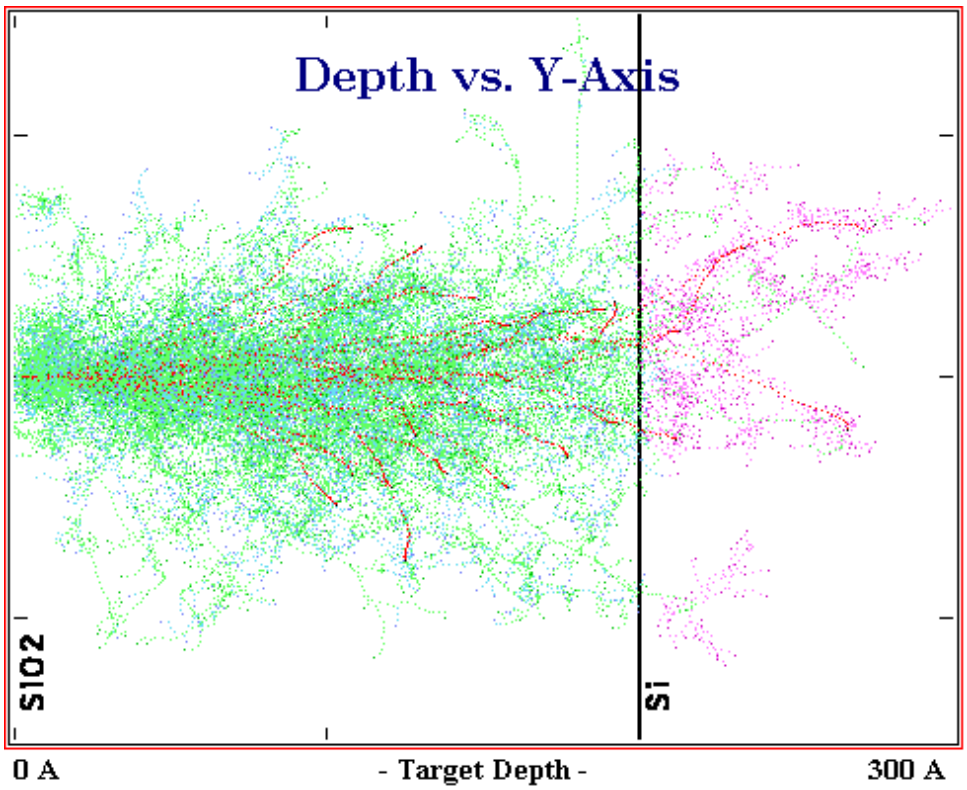


Figure 2.11: Typical SRIM cascades for a 12 keV Ge ion implantation in 20 nm thin SiO_2 layer grown on a Si wafer substrate (normal incidence) [192]. The colors indicate the incident Ge ions (red), the displaced oxygen (green) and Si atoms (blue) from the oxide and the displaced Si atoms from the Si substrate (magenta).

nent, layer thicknesses etc.), and also general target energy parameter have to be defined in a separate input file as summarized in Table 2.3. Therein, the *bulk binding energy* E_{BB} - which is often set to zero with good results - reduces the energy transfer to a recoil atom before it is set in motion. The energy to form a Frenkel pair (energy to relocate an interstitial atom far enough without immediate recombination) is considered in the *relocation threshold* E_{RTH}. The *cut-off energy* E_{CO} determines the threshold energy at which an atom or pseudoparticle in a collision cascade is stopped. It should be set as high as possible, as too low values would lead to very long needless computation times, but at least lower than other relevant energies (e.g., the surface binding energies).

According to a ternary element system including Ge, Si and O (Ge ion implantation in SiO_2), three *surface binding energies* (*SBE*'s) have to be defined. The *SBE* is a critical parameter as it determines the sputtering yield in the simulation (the sputtering yield is proportional to the inverse of the *SBE*). They are related to the actual surface atomic fractions c_j of the target atoms j variable ($1 \leq j \leq NCP$, the total number of components).

$$SBE_i = \sum_{j=1}^{NCP} SBV_{ij} \cdot c_j \tag{2.9}$$

Table 2.3: Structural density and energy parameter used for the TRIDYN simulation. Data for the heat of formation are necessary to calculate the surface binding energies.

parameter for simulation	in units of	value				
		Si	O	Ge		
atomic density of component	$(10^{22}/cm^3)$	4.98	8.31	4.43		
		E_{BB}	E_{RTH}	E_{CO}		
general target energy parameter	(eV)	0	8	4		
		Si	O	SiO_2	Ge	GeO_2
standard heat of	(kJ/mol)	450	249.2	-910.7	372	-580
formation $\Delta_f H^\circ$ [194]	(eV)	4.66	2.58	-9.44	3.86	-6.0

The matrix elements SBV_{ij} denote the interaction energies between atoms i and j (with $SBV_{ij} = SBV_{ji}$). This yields for the present system

$$\begin{pmatrix} SBE_{Ge} \\ SBE_{Si} \\ SBE_O \end{pmatrix} = \begin{pmatrix} SBV_{Ge,Ge} & SBV_{Ge,Si} & SBV_{Ge,O} \\ SBV_{Si,Ge} & SBV_{Si,Si} & SBV_{Si,O} \\ SBV_{O,Ge} & SBV_{O,Si} & SBV_{O,O} \end{pmatrix} \cdot \begin{pmatrix} c_{Ge} \\ c_{Si} \\ c_O \end{pmatrix} \quad .$$

Thus, besides (Ge, Ge) and (Si, Si) the target can have one solid-solid compound (Ge, Si) and two solid-gas compounds (Si, O)/(Ge, O). The SBV's can be obtained for the Si-Ge case from their enthalpies of formation and sublimation per molecule ΔH^f and ΔH^s, respectively. For $c_{Ge} = 1$ and $c_{Si} = 0$ and vice versa they are given in Table 2.3.

$$SBV_{Ge,Ge} = \Delta H^s_{Ge} = \mathbf{3.86\,eV} \quad \text{and} \quad SBV_{Si,Si} = \Delta H^s_{Si} = \mathbf{4.66\,eV} \tag{2.10}$$

Related to a Ge_nSi_m system the conservation of energy requires

$$n \cdot SBE_{Ge} + m \cdot SBE_{Si} = n \cdot \Delta H^s_{Ge} + m \cdot \Delta H^s_{Si} + \Delta H^f \tag{2.11}$$

which yields with $c_{Ge} = n/(n+m)$, $c_{Si} = m/(n+m)$, and Eq.(2.9)

$$\begin{aligned} SBV_{Ge,Si} = SBV_{Si,Ge} &= \frac{1}{2}(\Delta H^s_{Ge} + \Delta H^s_{Si}) + \frac{n+m}{2nm}\Delta H^f_{Si-Ge} \\ &\approx \frac{1}{2}(\Delta H^s_{Ge} + \Delta H^s_{Si}) = \mathbf{4.26\,eV} \end{aligned} \tag{2.12}$$

($\Delta H^s_{Si-Ge} \ll \Delta H^s_{Ge} < \Delta H^s_{Si}$ [195]). For the solid-gas compounds (Si,O and Ge,O) (e.g., $Si_nO_m = Si_1O_2$), one gets in analogy to Eq. (2.11)

$$n \cdot SBE_{Si} + m \cdot SBE_O = n \cdot \Delta H^s_{Si} + \Delta H^f_{SiO_2} + \frac{m}{2} \cdot \Delta H^{diss} \tag{2.13}$$

$$\text{and} \qquad SBV_{Si,O} = \frac{1}{2}\Delta^s H_{Si} + \frac{n+m}{2nm}\Delta^f H_{SiO_2} + \frac{n+m}{4n}\Delta^{diss} H_{O_2} \qquad (2.14)$$
$$= \frac{1}{2}\,4.66\,\text{eV} + \frac{3}{4}\,9.44\,\text{eV} + \frac{3}{4}\,2.58\,\text{eV}\cdot 2 \;=\; \mathbf{13.28\,eV} \quad .$$

In order to sputter a Si or O atom from the SiO_2 target an energy higher than the surface binding energies of

$$SBE_{Si} = SBE_{Si,Si}\cdot\frac{1}{3} + SBE_{Si,O}\cdot\frac{2}{3} \;=\; 10.4\,eV$$
$$SBE_{O} = SBE_{Si,O}\cdot\frac{1}{3} + SBE_{O,O}\cdot\frac{2}{3} \;=\; 4.43\,eV$$

is needed ($SBV_{O,O}$ is zero for gases). As a cross-check, the sum of the SBE's has to be equal to the total heat of atomization of SiO_2 $\Delta H^a_{SiO_2}$.

$$SBE_{Si} + 2\cdot SBE_O \;=\; \Delta H^a_{SiO_2} \;=\; (\Delta H^s_{Si} + 2\cdot\Delta H^{diss}_O) - \Delta H^f_{SiO_2}$$
$$10.4\,\text{eV} \;+\; 2\cdot 4.43\,\text{eV} = \;19.26\,\text{eV} \;=\; (4.66\,\text{eV} \;+\; 5.16\,\text{eV}) + \;9.44\,\text{eV}$$

In analogy to SiO_2, $SBE_{Ge,O} = \mathbf{10.3\,eV}$ can be obtained, which finally leads to the complete matrix of SBV's.

$$\begin{pmatrix} SBV_{Ge,Ge} & SBV_{Ge,Si} & SBV_{Ge,O} \\ SBV_{Si,Ge} & SBV_{Si,Si} & SBV_{Si,O} \\ SBV_{O,Ge} & SBV_{O,Si} & SBV_{O,O} \end{pmatrix} = \begin{pmatrix} 3.86\,\text{eV} & 4.26\,\text{eV} & 10.3\,\text{eV} \\ 4.26\,\text{eV} & 4.66\,\text{eV} & 13.28\,\text{eV} \\ 10.3\,\text{eV} & 13.28\,\text{eV} & 0 \end{pmatrix}$$

A TRIDYN simulation for a Si implantation in SiO_2 requires only the matrix elements $SBV_{Si,Si}$, $SBV_{Si,O}$, $SBV_{O,Si}$ and $SBV_{O,O}$. For a more detailed description of input parameters see the TRIDYN manual [196]. A validation of the sputtering yields is given in Ref. [119].

2.6 High fluence ion implantation in thin gate oxides and related effects

This chapter addresses the Si and Ge high fluence ion implantation carried out mainly in thermally grown 20 nm thin SiO_2 layers on p-Si substrates. Using the SRIM and TRIDYN codes for comparison (Fig. 2.12), Si and Ge ion profiles are discussed with respect to oxide swelling and surface erosion effects. In Figs. 2.13, 2.15 and 2.16 first structural results are shown according to high-resolution bright-field transmission electron microcopy (TEM) measurements. As a consequence of high fluence ion implantation, a substrate amorphization has been obtained and also a recrystallization which occurrs due to solid phase epitaxy during subsequent annealing.

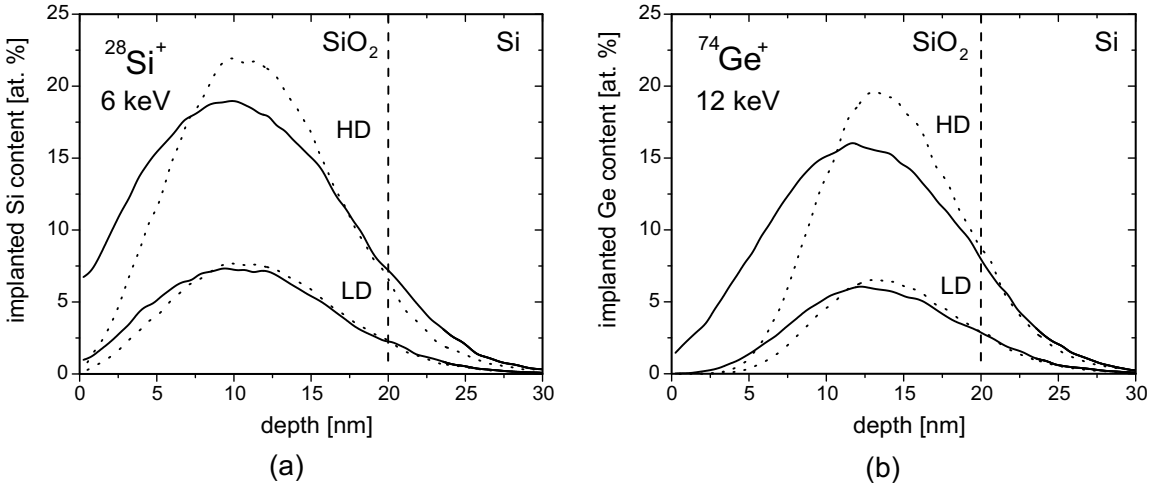


Figure 2.12: Simulated Si and Ge ion profiles in (a) and (b), respectively, according to the implantation parameter in Tab. 2.4. The TRIDYN (straight lines) and SRIM (dotted lines) results are shown for comparison. The initial position of the Si/SiO_2 interface is indicated.

Selecting suitable ion beam parameter

Aiming at memory device applications, the embedded NC's should be located as close as possible but well separated to the Si/SiO_2 interface to ensure a dominant charge exchange of the NC's with the Si substrate, not with the gate electrode. The ion fluences and energies were initially adjusted to achieve an impurity concentration in SiO_2 at the profile maximum of about 7 and 20 at.% more or less equal for both elements using the SRIM code; the calculated ion profiles for the SRIM and TRIDYN codes in Fig. 2.12 calculated for the selected beam parameter are summarized in Tab. 2.4. Additionally, a similar Si or Ge concentration at the position the Si/SiO_2 interface was required to get a comparable and moderate amount of impurity atoms there. As a consequence, in both cases the ion profile maximum comes to rest in the oxide center (Si-II) or a little bit closer to the Si substrate (Ge-II).

Oxide swelling and surface erosion

Considering dynamic changes in the matrix composition during the ion implantation using TRIDYN instead of SRIM, the impurity profile calculation result in broader Si and Ge distributions (Fig. 2.12) with a lower peak concentration shifted slightly toward the oxide surface (cf. x_c^{stat} and x_c^{dyn} in Table 2.4). These effects become more and more significant if the achieved impurity concentration at the profile maximum is higher than about 10 at.%. In case of the high fluence ($2\times10^{16}\,cm^{-2}$) Si^+ implantation the abundant excess of Si in SiO_2 leads to a considerable oxide swelling of 1.4 nm as predicted by TRIDYN (negative surface recession *SFRC*). Figure 2.14(a) shows the respective results more clearly. The effect of swelling causes a clear shift of the Si/SiO_2 interface position

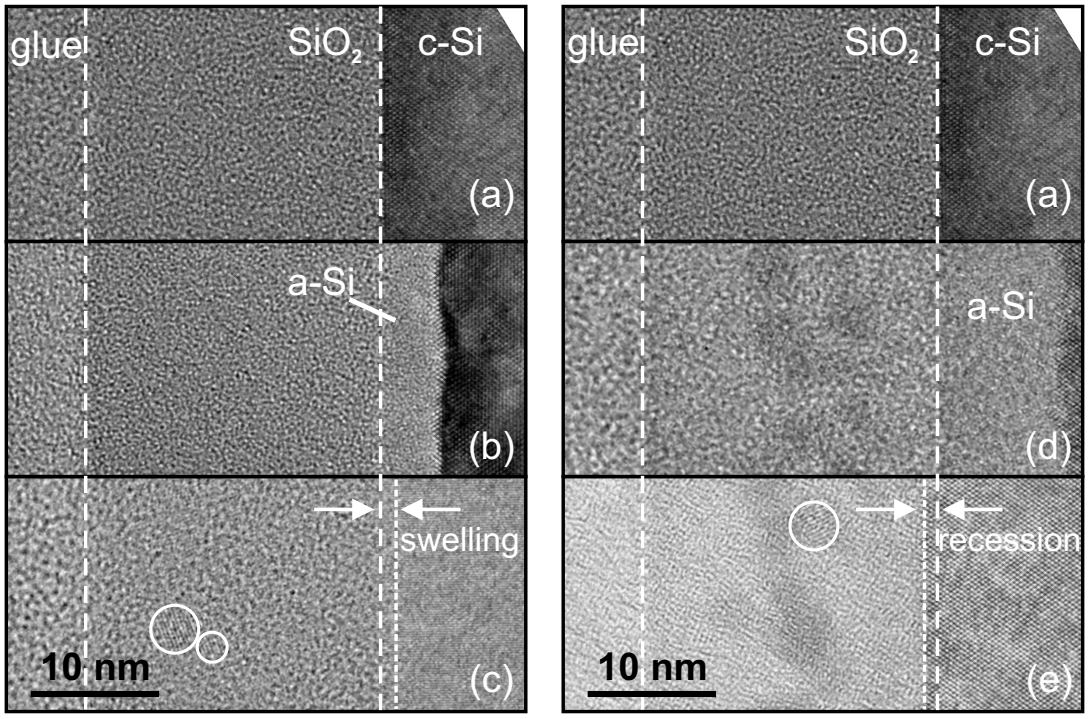


Figure 2.13: Cross section TEM micrographs for virgin (a), 6 keV Si (b-c) and 12 keV Ge (d-e) ion implanted oxides (at $2\times10^{16}\,\mathrm{cm}^{-2}$ and $1.5\times10^{16}\,\mathrm{cm}^{-2}$, respectively) before [(b), (d)] and after annealing [(c), (e)]. The annealing was carried out at 1050°C (Si) and 950°C (Ge) both for 30 s in ultra-pure Ar. In (d) tiny ($\lesssim 2$ nm) Ge precipitates were obtained as indicated by the shaded areas even for the as-implanted state. Lattice fringes in (c) and (e) confirm the existence of Si and Ge NC's ($d_{nc} \approx 3$ nm) in the oxide after annealing, respectively.

with respect to the oxide surface, which fits approximately to the experimental observation in Fig. 2.13(c). Focussing only on the introduction of Si during the implantation process neglecting any oxide surface erosion (sputtering), the swelling of the oxide would come up to 4 nm. However, the actual *SFRC* data obtained by TRIDYN (Tab. 2.4) represent the balance between oxide swelling and oxide surface erosion. The latter effect is related to a sputtering yield of the incident ions during the ion implantation; an oxide atom can be released to the ambience if the collision cascades in the oxide reaches the oxide surface. Thus, a negative *SFRC* value means that the oxide swelling dominates over the surface erosion. In case of the Ge ion implantation [Fig. 2.14(b)] both effects are balanced ($SFRC = 0$) due to a higher sputtering yield at the oxide surface for incident Ge ions than of Si ions. A higher stopping power of Ge in SiO_2 than of Si [see Fig. 2.10] indicates a higher energy transfer to Si and O matrix atoms with an increased probability to release an oxide atom from the oxide surface. The surface recession clearly obtained by TEM in Fig. 2.13(e) is most likely related to a considerable Ge loss during the cleaning and annealing processing, which reduces actually the amount of Ge included in the oxide (less oxide swelling). For details to the Ge loss effect see chapter 5.

Table 2.4: Energy, fluence, and profile parameter for Si^+ and Ge^+ implantation in 20 nm thin oxide layers (see the corresponding profiles in Fig. 2.12). R_p denotes the average projected range as predicted by SRIM. The x_c's stand for the center positions (maxima) obtained from a Gaussian fit of the ion profiles (Fig. 2.12) with respect to the oxide surface. The results for the SRIM and TRIDYN calculations are indicated by the superscripts (*stat*) and (*dyn*), respectively. The surface recession (*SFRC*) - data given by the TRIDYN program - denotes the balance between oxide swelling by impurity accumulation in the target during the ion implantation and surface sputtering.

initial beam parameter			SRIM		TRIDYN	
ion	energy [keV]	fluence [$\times 10^{16}\,cm^{-2}$]	R_p [nm]	x_c^{stat} [nm]	x_c^{dyn} [nm]	*SFRC* [nm]
$^{28}Si^+$	6	0.7	11.5	11.2	10.5	-0.5
		2.0			10.0	-1.4
$^{74}Ge^+$	12	0.5	14.4	14.1	13.3	0.0
		1.5			12.4	0.0

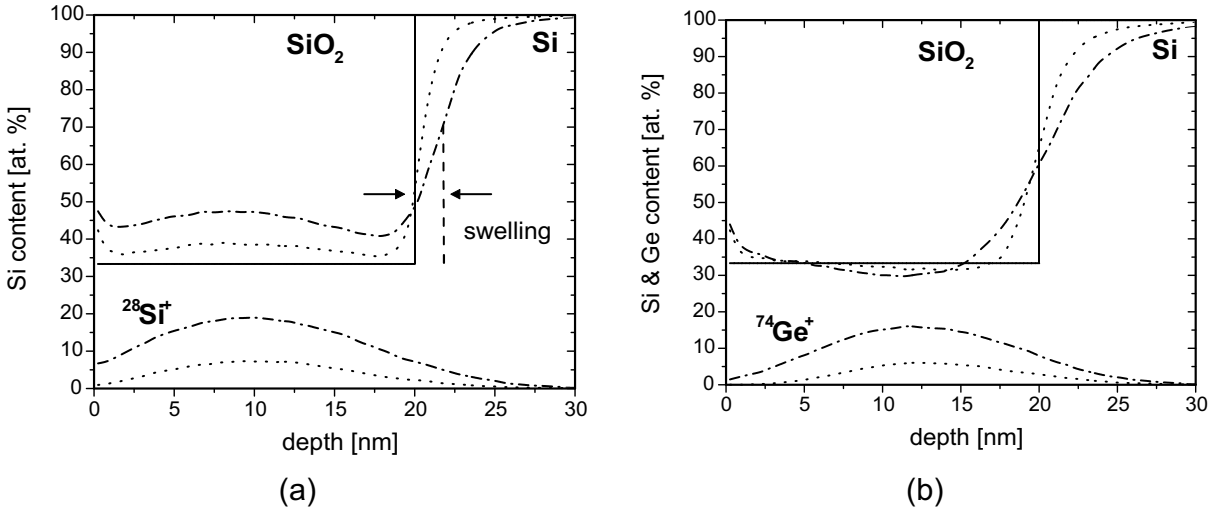


Figure 2.14: Total Si and implanted ^{28}Si (a) and ^{74}Ge content (b) in 20 nm SiO_2 for different fluences according to Tab. 2.4 obtained using the TRIDYN code.

Table 2.5: Parameter for Ge and Si ion implantation varying the ion energy and oxide thickness and the subsequent annealing. For the respective ion profiles and structural results see the Figs. 2.15 - 2.18. The average projected ion range R_p is deduced from SRIM calculations.

d_{ox} [nm]	ion	energy [keV]	fluence [$\times 10^{16}\,\mathrm{cm}^{-2}$]	R_p [nm]	annealing
8.5	$^{74}Ge^+$	3	0.5	6.0	950°C, 30 s
20	$^{28}Si^+$	10	2.0	17.4	1050°C, 30 s
	$^{74}Ge^+$	18	1.5	17.6	950°C, 30 s
100	$^{74}Ge^+$	70	3.0	53.2	950°C, 30 s/ 1050°C, 120 s

Substrate amorphization and Si/SiO_2 interface recovery

As shown in Fig. 2.12 a part of the implanted Si and Ge ions exceeds the Si/SiO_2 interface and penetrate the crystalline Si substrate. Primary and recoiled Si atoms from the collision cascade cause an amorphization of a thin Si layer due to multiple atomic displacements. This effect is confirmed by TEM studies for the as-implanted case in Fig. 2.13(b) and (d). These displacements cause also a considerable mixing of the Si/SiO_2 interface during the ion implantation as shown in Fig. 2.14. Some silicon and oxygen atoms are recoiled from the SiO_2 network into the Si substrate and Si atoms from the Si substrate back into the oxide. This interface mixing varies with the ion fluence and element (Si or Ge) as can be seen by the different gradients of the increasing Si content at the Si/SiO_2 interface in Fig. 2.14. In Fig. 2.15 the damage in the implanted samples is plotted for different Si ion energies. About 0.3 - 0.5 displacements per atom (*dpa*) are needed to yield a full amorphization of the Si substrate. Amorphization occurs if a a critical value of energy per unit volume of about 5×10^{23} eV/cm^3 [197], i.e. 10 eV/atom or 0.4 dpa (assuming a displacement energy of 25 eV/atom), is deposited in the crystalline Si substrate. This corresponds to a displacement of at least each second or third Si atom on average at a certain substrate depth. But during a subsequent annealing, which should be performed at T > 600°C, solid phase epitaxy [198, 199] occurs with a rapid recrystallization of the a-Si layer [Fig. 2.13(c) and (e)]. Additionally, an atomically flat Si/SiO_2 interface regrows.

As shown in Fig. 2.13 the Si and Ge NC's are mainly produced at the ion profile maximum in the oxide center. In order to locate the NC's closer to the Si/SiO_2 interface an additional implantation series was carried out with increased ion energies, namely 10 keV Si^+ and 18 keV Ge^+ (see Tab. 2.5 for details). This yields a broader impurity distribution as shown for the Si^+ case in Fig. 2.15, for instance, with a higher concentration of implanted ions at the Si/SiO_2 interface. As a consequence the amorphous region in the Si substrate gains further depth. In fact, the Si NC's detected in Fig. 2.16(a) are placed in the oxide much closer to the Si substrate. But on the other hand, the high impact of the implanted impurities at the Si/SiO_2 interface inhibits a flat reconstruction during

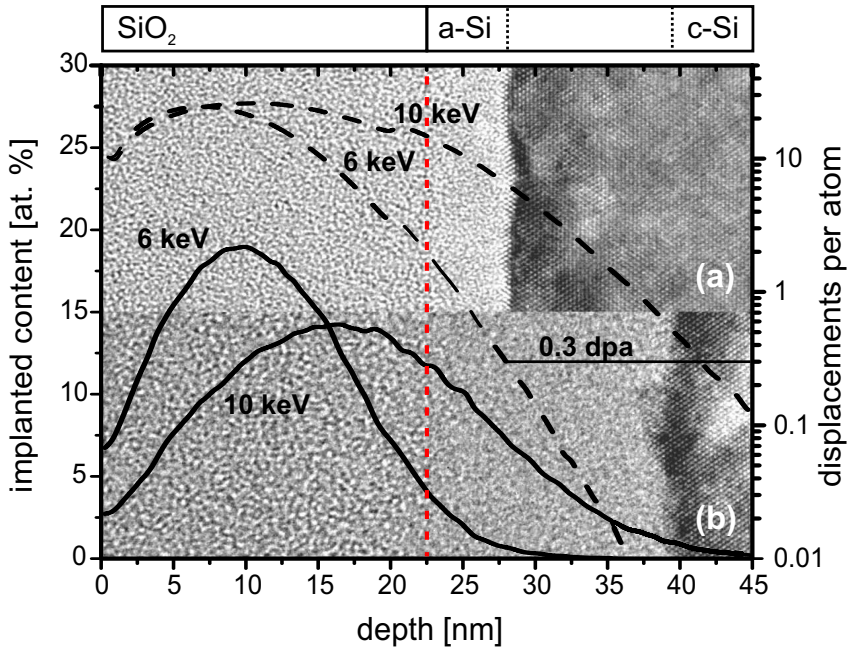


Figure 2.15: Content of implanted Si impurities (closed lines, left ordinate, using the TRIDYN code) and related displacements per atom rate (dashed lines, right ordinate, using the SRIM code) as a function of the oxide and Si substrate depth. The graphs are superimposed to cross section TEM bright field images for (a) 6 keV and (b) 10 keV Si^+, 2×10^{16} cm^{-2} implants revealing the as-implanted state. Beyond the 22.5 nm thin thermal oxide (including oxide swelling of about 1.5 nm) about 5 to 15 nm of the crystalline Si substrate got amorphized due to atomic collision by the implanted ions and related recoils.

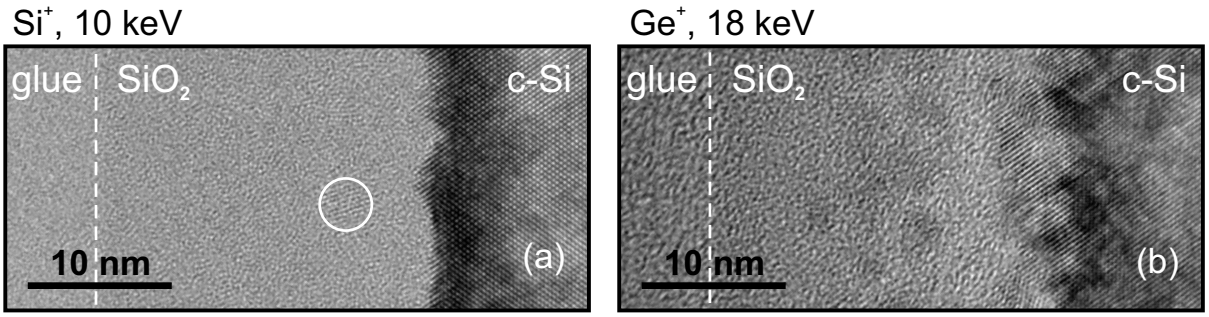


Figure 2.16: Cross section TEM micrographs in high resolution for (a) 10 keV Si, 2×10^{16} cm^{-2} and (b) 18 keV Ge, 1.5×10^{16} cm^{-2} ion implantation in 20 nm thin SiO_2 layers. The samples were annealed at 1050 and 950°C for 30 s, respectively (see Tab. 2.5). For (b) no significant structural changes were obtained after 1050°C annealing in comparison to the shown image.

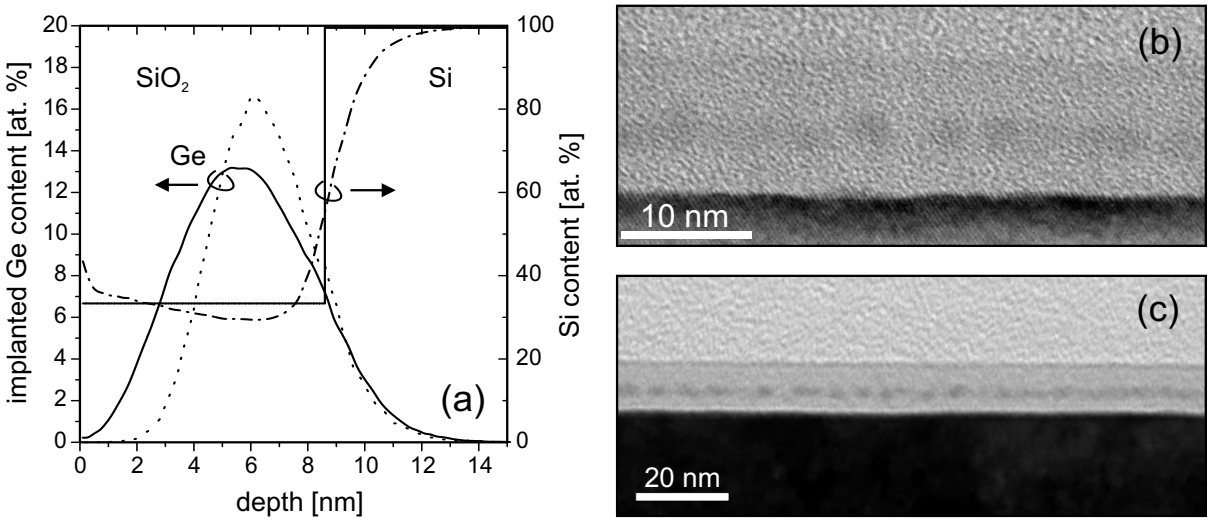


Figure 2.17: (a) As-implanted Ge content as predicted by SRIM (dotted curve) and TRI-DYN (straight curve) calculations (left ordinate). The implantation was carried out for 3 keV Ge ions at a $5{\times}10^{15}\,\mathrm{cm}^{-2}$ fluence in 8.5 nm ultra-thin gate oxide (see Tab. 2.5). The Si content shown before and after implantation (straight and broken line, right ordinate) reveals a considerable mixing of the Si/SiO_2 interface due to the ion bombardment. The bright-field cross-section TEM micrographs in (b) and (c) confirm the synthesis of a Ge NC layer in the oxide during annealing in different magnification.

annealing. The resulting high interface roughness is incompatible to state-of-the-art microelectronic device specifications, where a flat interface is demanded with a precision of about 0.1 nm for the tunneling oxide thickness. Due to the increased ion impact a higher concentration of remaining dislocations can be expected within the Si substrate. Such structural misfits have a crucial impact on the Si/SiO_2 interface trap density and thus on the transistor device characteristics. A higher annealing temperature should lower the interface roughness, but to the expense of the dissolution of those NC which are located close to the interface. Notice the structural disorder in case of the respective Ge^+ implantation shown in Fig. 2.16(b). After annealing Ge or mixed Si_xGe_{1-x} NC's form at the Si/SiO_2 interface directly attached to the Si substrate or a Si_xGe_{1-x} "strained layer". As a consequence for the low energy ion implantation concept, the ion energy can be considered as a rather confined parameter due to the inherently broad impurity distribution in the oxide, especially if the structural properties have to satisfy the requirements of future memory device concepts.

Synthesis of Ge NC's in 8.5 and 100 nm thin oxide layers

With respect to the demands of future memory devices, realizing even shorter programming times, at even lower operation voltages or possibly utilizing single electron effects, the Ge ion implantation was also performed in much thinner gate oxides of 8.5 nm size. As shown in the TEM micrographs in Fig. 2.17(b) and (c) also for this very critical case

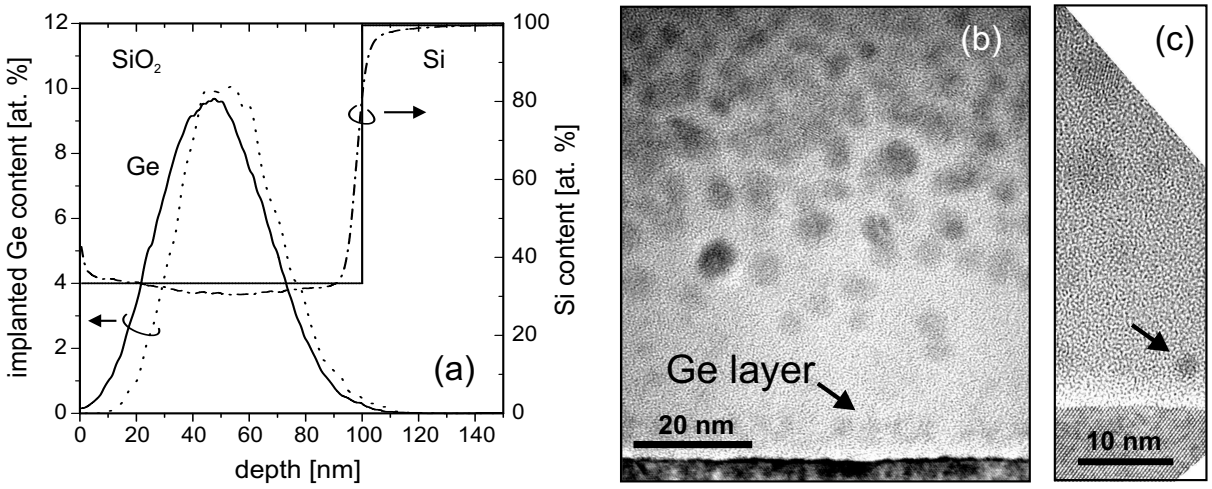


Figure 2.18: (a) Ge content for the 70 keV ^{74}Ge, $3\times10^{16}\,cm^{-2}$ ion implantation in 100 nm SiO_2 (legend similar to Fig. 2.17). Bright-field cross-section TEM micrographs for 950°C, 30 s and 1050°C, 120 s annealing in (b) and (c), respectively (see also Tab. 2.5).

the ion beam synthesis of Ge NC's succeeded. The ion implantation was carried out at a moderate implantation fluence of $5\times10^{15}\,cm^{-2}$ which yields a considerable Ge concentration in the oxide of about 15 at.%. The respective Ge and Si profiles from SRIM and TRIDYN calculations are shown in Fig. 2.17(a). A single layer of tiny Ge NC's of about 2 nm size is achieved embedded in SiO_2 which is located slightly closer to the Si substrate than to the oxide surface. The position of NC's follows the as-implanted Ge distribution as predicted by TRIDYN [Fig. 2.17(a)]. But the NC's are smaller than one would expect from the significant Ge excess in the oxide. A zone between the Ge NC's and the Si substrate forms denuded of Ge. This is most likely related to (i) a loss of Ge during cleaning and annealing and (ii) a Ge depletion due to Ge diffusion towards the Si substrate. The Si substrate works as a sink for Ge.

In order to study the differences and similarities of NC synthesis in very thin oxides in comparison to much thicker ones, the ion beam synthesis of Ge NC's was also performed in 100 nm thick SiO_2 layers. In Fig. 2.18 the respective theoretical and structural results are shown according to the implantation and annealing parameter summarized in Tab. 2.5. Dynamic composition changes affecting the profile shape are less pronounced compared to implantation in very thin oxides as the Ge content reaches only about 10 at.% at its maximum. After annealing Ge NC's are mainly prepared in the oxide center but filling most of the oxide volume due to the broad ion distribution in SiO_2 as shown in Fig. 2.18(a). The size of the NC's ranges between 2 and 6 nm. Additionally some Ge accumulates in the oxide close to the Si/SiO_2 interface forming a layer of Ge precipitates or nanocrystals in vicinity to the Si substrate during the thermal treatment as shown in the TEM micrographs of Figs. 2.18(b) and (c) with a weak contrast after 950°C, 30 s annealing and slightly clearer after 1050°C, 120 s annealing, respectively. Also in this case, this effect is related to the previously discussed redistribution of Ge (see chapter 5 for details). Also 35 keV $^{28}Si^+$ implantations were performed in 100 nm with a similar

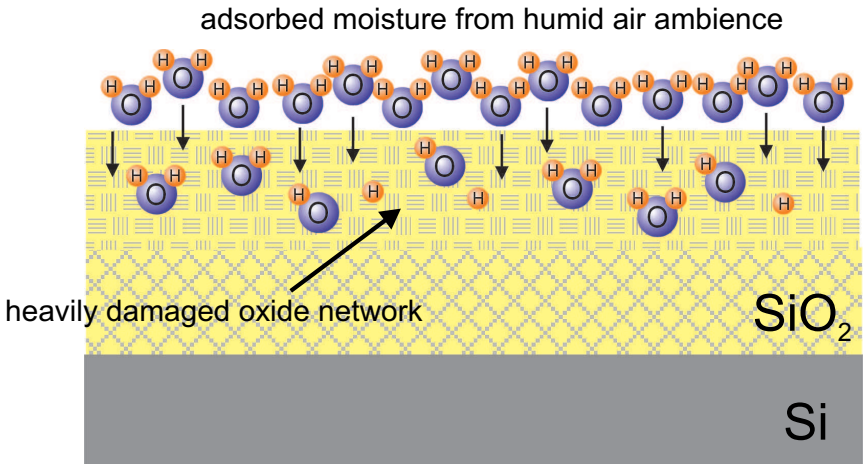


Figure 2.19: Humidity adsorbed at the oxide surface provides water molecules which penetrate the heavily damaged oxide during exposure to normal air condition.

maximum concentration and profile shape as done for the Ge implantation. But on these sample no proof of Si NC's succeeded by conventional bright-field TEM imaging. As no additional structural information has been obtained from these samples, respective results are not shown. The implantations in 8.5 and 100 nm were prepared only for comparative structural studies and have not been taken into account for electrical analysis in this thesis.

2.7 The impact of humidity on IBS of NC's in thin oxide layers

Ion implantation creates a significant amount of displaced atoms and broken bonds in the SiO_4 tetrahedra network close to the oxide surface (in case noble gas ions are implanted into the oxide, actually the formation of bubbles inside the oxide was observed [200, 201]). The damage introduces pathways for moisture and other chemicals into the oxide [187]. During sample exposure to humid air after ion implantation and/or sample cleaning during wafer processing, water adsorbs at the oxide surface and penetrates into the disturbed oxide as H_2O (see Fig. 2.19) or after dissociation as OH^- and H^+ (H_3O^+) molecules. As known from gas solubility measurements [202], molecules with a diameter smaller than 3 Å- which is valid for OH^-, H_3O^+, and H_2O (size of about 2.8 Å) [203] - are able to penetrate into SiO_2 layers (fused silica). Even more this should be possible for a pre-damaged network close to the oxide surface. Thus, these molecules have been considered as "point-like" impurities diffusing through the oxide [187]. As a consequence of the humidity penetration (as e.g. H_2O or OH^-), the hydrogen (and obviously also the oxygen) concentration close to the oxide surface is enhanced as reported in Refs. [187] and [200] which decays with oxide depth in a diffusion-like profile manner. The penetration may

exceed more than 30 nm in the oxide depth [187]. The hydration depends on the relative humidity, the time of ambience exposure, and on the fluence of ion implantation (degree of damage) [204].

Considering the case of low energy ion implantation, the Si or Ge impurity profiles overlap with the region of increased hydrogen and oxygen concentration. Thus, chemical reactions have to be taken into account which reduce the Si and Ge excess in the oxide available for Si NC formation and growth (M stands for Si or Ge).

$$2\,\mathrm{M} + 2\,\mathrm{H_2O} \quad \longrightarrow \quad 2\,\mathrm{M} + 2\,\mathrm{OH^-} + 2\,\mathrm{H^+} \quad \longrightarrow \quad \mathrm{MH_4} + \mathrm{MO_2} \tag{2.15}$$

During the required annealing treatment the impurities M oxidize to MO_2 (e.g., SiO_2) fitting to the oxide network or to other compounds like $M(OH)_x$ (hydroxides) or MO (monoxides). Volatile GeH_4 is discussed to be responsible for a significant Ge redistribution during annealing [178, 179, 186, 188]. Schmidt *at al.* [187] implanted Si^+, Ge^+, and Sn^+ in 100 nm SiO_2 to different fluences but with a similar projected range ($R_p \approx 20$ nm) to study the role of ion mass and implantation fluence on the hydration of SiO_2. In these samples the hydrogen content - obtained by nuclear reaction analysis (NRA) - decays from about 15 at.% very close to the surface to about 5 at.% at 40 nm oxide depth. An as-grown dry oxide (thermally grown using O_2), for comparison, has a constant concentration of 0.5 at.% which increases by about 2 at.% due to wet chemical cleaning (sensitivity limit of NRA is 0.02 at.%). As mentioned by the authors [187], from a structural point of view the penetration of water molecules into the oxide occurs if each third or fourth bond has been broken at an average. Thus, each SiO_4 tetrahedra has to be affected only once by the penetrating ions.

In general, several intrinsic defects have been identified to occur in amorphous SiO_2 layers (see, e.g., Ref. [205]). The most prominent are the oxygen-vacancy center (e.g., the neutral $O_3{\equiv}Si\text{-}Si{\equiv}O_3$) and the non-bridging oxygen-hole (NBOH) center ($O_3{\equiv}Si\text{-}O$). Both are generated in SiO_2 during ion implantation by nuclear displacements and electronic energy loss (ionization), respectively [205]. Also a densification of the oxide has been reported, which indicates macroscopic changes in the SiO_2 network by implantation as well, leading to an increased refractive index of the oxide and a higher etch rate [205, 206]. Four and more membered SiO_4 tetrahedra rings reconfigure to strained three membered rings (3 Si and 3 O atoms in a loop) in irradiated material. As a consequence in these oxides the bridging bond angle is reduced in comparison to non-treated samples [205, 207]. Michalske and Freiman reported [204, 208] that water is able to attack strained Si-O-Si bonds. In absence of strain, the silicon oxygen bond is inert to H_2O and other chemicals. But if either the Si-O-Si or the O-Si-O bond angles are changed the reactivity is increased. Strained Si-O-Si bonds in the three-membered ring structures break up if water molecules are adsorbed at the oxide surface. As a consequence OH^- and H^+ react with the open bonds to build silanol groups ($\equiv$Si-OH) at the point of rupture which delivers stress to deeper Si-O bonds. Thus, the strained Si-O bonds located in the compacted oxide region allow adsorbed H_2O molecules an easier access into deeper oxide regions. In contrary, the diffusion of larger oxygen molecules (O_2) through SiO_2 is less probable (3.2 Å molecule diameter) [202]. O_2 is more inert to the oxide network and

diffuses as an interstitial molecule [209]. Atomic collision- and ionization-induced structural defects caused by the ion implantation need a temperature similar to that of original oxide growth or at least more than 800°C in the subsequent annealing, respectively, to achieve structural properties equivalent to that before the ion bombardment [210].

Thus, a penetration of the oxide with humidity can hardly be influenced or avoided once the damaged or implanted oxide is exposed to humid air ambience. The treated sample has to be annealed inside the implantation chamber or a covering layer has to be deposited without breaking the vacuum conditions after the ion implantation. But both features were not available for the present thesis due to technical constraints.

2.8 Nanocrystals under thermal treatment

The thermal annealing is an essential process for the ion beam synthesis of nanocrystals. Two effects are frequently discussed aiming at the thermal treatment of NC's, a decreased melting-point of nanoparticles and their limited oxidation. These topics are not included in the discussion of the thesis results. But they are of general interest for the preparation of nanoparticles (e.g. concerning the TEM detection limits, consequences for the ripening behavior, or size limits for NC related photoluminescence) and are mentioned briefly for the sake of completeness.

Nanoparticle size-dependent melting point

On small particles with a size of 20 nm and below, their physical and chemical properties deviate from those of their bulk materials. A non-negligible part of nanoparticle atoms are located at its surface. Following roughly the surface-phonon instability model, a simple formula is reported which describes the size-dependent melting temperature T_m of small nanoparticles [211, 212].

$$\frac{T_m}{T_0} \simeq 1 - \frac{\beta}{d} \tag{2.16}$$

T_0 denotes the bulk melting temperature, d the particle diameter, and β a constant material parameter related to the interatomic distance [212, 213]. For Si NC's in the range of 2 - 3 nm T_m is obtained to 227°C (bulk melting temperature of silicon is 1414°C) [213] which implies that these NC's are liquid at typical annealing temperatures of 1050°C. Data extrapolations reveal that smaller particles of about 1 nm size should be liquid even at room temperature. In fact, in TEM studies their crystalline reflexes disappear with decreasing particle size [213]. Yu *et al.* showed that Si NC's lose their bulk diamond structure if they get smaller than 2.3 - 2.7 nm [214]. For silica-encapsulated Au NC's this structural transition happens at $T_m \approx 600$ - 800 K (300 - 500°C) at a particle size of about 2.5 nm [215]. Ge NC's of the same size show a significant melting-point hysteresis embedded in SiO_2 spanning about 470 K around its bulk value [216]. The actual T_m of these particles was determined to 1077°C which is much higher than for bulk Ge (938.25°C)! As a consequence, it can not be decided whether the Ge NC's should be considered as solid or liquid at annealing temperatures of 950 - 1050°C as applied in the

present work. It should be mentioned that the melting point can be different for free NC's located at a sample surface to those which are embedded in SiO_2.

Self-limiting oxidation of Si and Ge NC's

For a flat Si surface the growth of an oxide layer is described by the classical Deal-Grove model [217]. In contradiction to this theory, the oxidation rate decreases for curved Si surfaces with decreasing particle size [218]. The self-limiting oxidation of small Si NC's was attributed to increasing stress at the Si/SiO_2 interface due to the volume expansion from Si (20 $Å^3$) to SiO_2 (45 $Å^3$) during the oxide growth [219, 220]. But as reported by Scheer *at al.* [221] the compressive stress is relieved at annealing temperatures in the range of 1000°C and above due to a viscous flow of SiO_2. As a consequence the validity of the self-limitation effect for the present experiments is questionable as the annealing of Si NC containing oxides is usually performed at 1050°C. Moreover, the stress due to volume expansion is reduced by the injection of Si self-interstitials into the Si nanoparticle [222]. This effect is well known discussing the formation of point defects and diffusion processes in bulk Si [223]. However, the self-limiting oxidation was reported for Si NC's fabricated by ultra-low energy ion implantation [224]. Also free 5 nm Ge NC's on SiO_2, which are prepared by ion beam synthesis in SiO_2 and subsequent selective oxide etching, are supposed to be stable under ambient atmospheric conditions at room temperature due to a similar effect [225].

2.9 Sample preparation with optimized annealing conditions

Specifications of ion implantation

The low energy ion implantations ($E < 30$ keV) were performed at the Foschungszentrum Dresden-Rossendorf (FZD) using a Danfysik DK - 1090 implanter. A double lens system (ion optical collection and dispersion) connected to the beamline (see Fig. 2.20) enables a decelerated ion beam with energies of 30 keV down to about 1 keV with a precision of $\pm\,0.1$ keV [226]. The ion optical extension provides a 150 mm diameter implantation area with a fluence inhomogeneity better than 5 % over 125 mm diameter. For the Ge^+ implantations a standard solid-state ion source is used. In order to enable high-fluence Si^+ implantations with ion currents up to 200 μA, a SiF_4 gas source was installed for this project. Using this source a typical $7\times10^{15}\,cm^{-2}$ Si^+ implantation is realized in only 20 min, for instance. The implantations were carried out mainly in 8" (200 mm) p-Si wafers already covered with 20 nm or 100 nm thin thermally grown gate oxide layers as provided by Infineon AG Dresden which is here gratefully acknowledged. The $^{28}Si^+$ implantations were all performed at the FZD and the $^{74}Ge^+$ implantations both at Infineon Dresden and FZD for comparison.

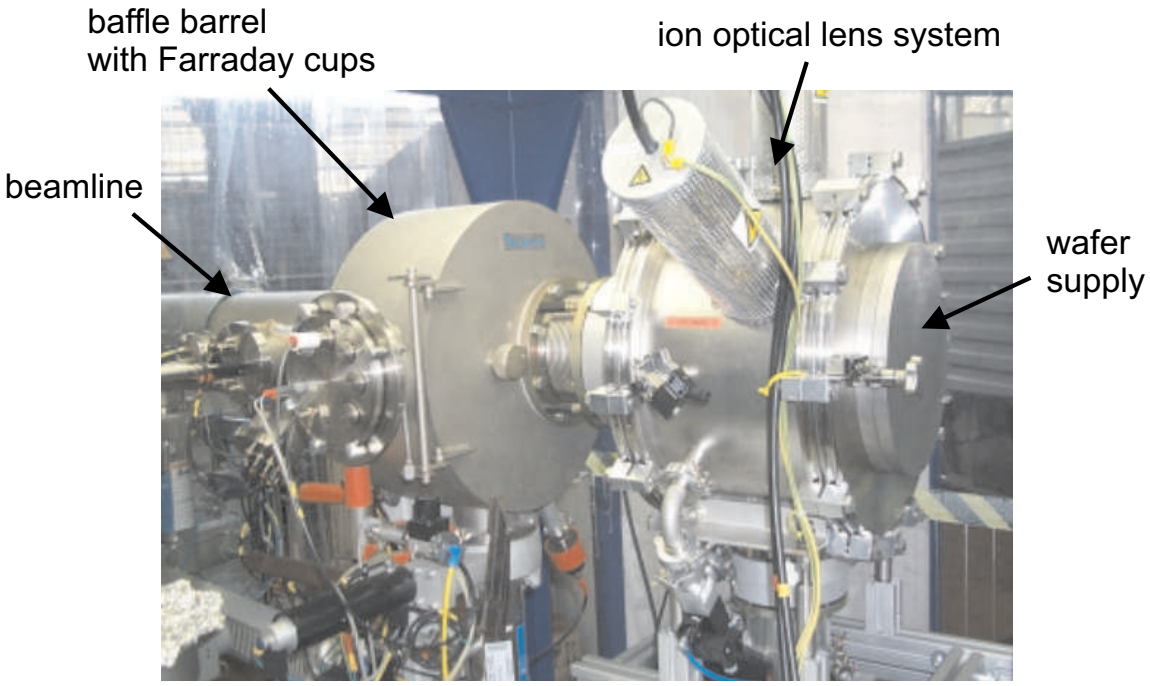


Figure 2.20: Ion optical deceleration unit fixed at the entrance of the Danfysik DK-1090 ion implanter beamline. The fluence is traced by Faraday cups. The holder is suitable to carry single wafers up to 8" size.

Avoiding contaminations from sample processing

During the ion implantation processing vacuum conditions were realized with a residual partial pressure of 1 - 5×10^{-6} mbar in the beamline related mainly to N_2. A low vacuum pressure is demanded to reduce the probability of ions interactions with residual gas atoms. Neutralized beam species are not decelerated and cause, thus, an energy contamination leading to an impurity profile extensions to substrate depth. This effect has been checked to apply approximately to less than or equal 0.1 - 1 % of the entire implanted fluence. For a singly charged Si ion beam ($^{28}Si^{+}$) a cross-contamination with doubly charged iron ions ($^{56}Fe^{2+}$) has to be taken into account. In order to avoid crucial metal contaminations some metal components in the ion source (mainly apertures) were replaced. After the reconfiguration the concentration of contaminating elements was checked by total-reflection x-ray fluorescence (TXRF) measurements. Inclusive wafer handling a CMOS compatible process level was achieved comparable to that defined in the microelectronic industry (e.g., $N_{Fe} < 2\times10^{11}cm^{-2}$, $N_{Cu} < 2\times10^{10}cm^{-2}$, and $N_{Al} < 10^{12}cm^{-2}$). Handling means that after implantation the wafer is carried in a closed box into in the clean-room area (class 100) still mounted on the holder but exposed to normal air conditions. There, the wafer is separated in $2\times,2$ cm^2 chips which are subsequently treated by a standard "Piranha" H_2O_2/H_2SO_4 cleaning procedure including rinsing in deionized water before annealing [227]. Effects on shallow ion profiles in SiO_2 from wet chemical cleaning processes are discussed in chapter 5.

Thermal processing

The thermal treatment necessary for oxide recovery and nanocrystal formation is carried out by rapid thermal annealing (RTA) using a Addax XM - A4 system. The quartz glas chamber provides short high temperature annealing steps at normal pressure (950 - 1150°C for $t \leq 120$ s, for instance, and $T = 1200$°C for 3 min at maximum). The allowed total thermal budget for state-of-the-art memory device fabrication is very restricted. An optimized transistor devices performance demands sensitively adjusted shallow doping profiles. Thus, the annealing temperature has to be as low as possible to conserve this state. But on the other hand, an oxide reconstruction and also the NC formation need annealing temperatures of $T \gg 900$°C (950 - 1050°C for Ge and $T \geq 1050$°C for Si NC formation). Therefore, the RTA treatment is the method of choice. The annealing process was performed first of all purging the chamber with a N_2/Ar gas mixture for 180 s and additionally for 120 s switched to Ar only. Then, the temperature is ramped to the desired value with 50 K/s and held for a specified time (here mainly 30 - 120 s). After that the heating is switched off and the sample cools down within 120 s waiting time followed by a chamber purge for 60 s. During the heating period the gas flow is reduced from 4 slm (standard liter per minute) to 2 slm to avoid sample cooling in the critical phase.

Annealing ambience adjustment

As discussed in chapter 2.7 after ion implantation water from adsorbed moisture is able to penetrate the damaged oxide. During subsequent annealing these oxidants soaking the SiO_2 and additionally oxygen from the annealing ambience/gas (mainly from residual H_2O) oxidize and therefore reduce the free amount of Si or Ge available for NC formation and growth. This loss has to be compensated by an implantation with higher fluences with negative impact on the oxide, Si substrate, and Si/SiO_2 interface recovery. Additionally, due to oxidation of Si and Ge a parasitic oxide growth has to be taken into account. All these effects have influences on the device reproducibility with respect to oxide thickness, the NC distribution and size. As shown in chapter 2.3 for very high Si or Ge excess in SiO_2 the formation of a buried layer in SiO_2 becomes possible (see Fig. 2.1) or at least of electrically or structurally linked vermicular nanostructures in SiO_2 after spinodal decomposition during annealing [114]. The use of increased fluences for loss compensation is contradictory to the idea of isolated NC's in a NC based memory device. As a consequence the amount of oxidants has to be restricted as much as possible in order to reduce the implanted fluence necessary for NC formation to a moderate value. Two sources for oxidants are distinguished, namely the intrinsic and the extrinsic one.

Intrinsic source Humidity (water) adsorbs on the oxide surface as the wafer is exposed to normal air after the ion implantation (see previous chapter). Subsequently, it is able to penetrate the damaged porous-like oxide region close to the surface. An in-situ annealing in the implantation chamber would solve this problem, but such a heating system is not yet available at modern implanter equipments. The combination of high

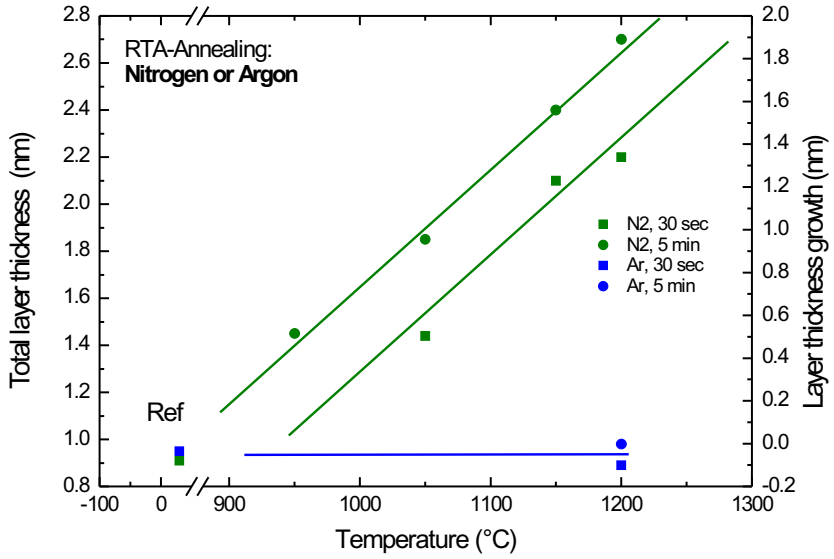


Figure 2.21: Influence of the ambience on the oxide layer growth on bare Si wafers during high temperature RTA treatment at low partial pressure of oxygen with the use of an AERONEX gas purifier. The layer thicknesses were measured by ellipsometry.

voltage areas with wafer heating including special isolations is problematic and needs significant expense. The subsequent wet chemical cleaning - needed after wafer implantation and handling - increases the total humidity content in the oxide just marginally [187]. With respect to humidity adsorption, the oxide surface is already conditioned right after a short air exposure.

Extrinsic source Oxidants present in the annealing gas or chamber during the thermal treatment are also critical for the ion beam synthesis of NC's. There, a rapid thermal annealing (RTA) process benefits from the short exposure time and the small chamber volume. Purging the chamber before processing sufficiently, the main supply of oxygen during the heating period comes from the annealing gas. Ar and N_2 were considered as suitable process gases with a preference for the former.

In order to reduce the oxygen contamination in the annealing ambience, an Aeronex gas purifier was implemented into the gas supply path to improve the gas quality - according to manufacturer information - from 5.0 to 9.0 grade (99.999 % to 99.9999999 %, i.e. from $\leq$10 ppm to $\leq$1 ppb) with respect to oxidizing moisture components (e.g., O_2, H_2O). The actual quality of the annealing ambience was qualified by means of a bare Si wafer. After a chemical etch of the native oxide in buffered HF the clean surface was exposed to purified Ar or N_2 gas during a thermal treatment at temperatures between 950 and 1200°C for 30 and 5 min. As shown in Fig. 2.21 annealing in N_2 leads to a considerable layer growth. Etching in HF solutions was effectless on this layer. Thus, the formation of an (oxy-)nitride-like layer on Si was supposed. The absence of SiO_2, especially in

case of Ar gas annealing, indicates that the purification of the annealing works efficiently with respect to oxygen or oxygen containing components. In agreement to the present result, an absorption of nitrogen in oxides containing Si nanocrystals was reported for the annealing in N_2 ambience at 950°C [141]. Nitrogen accumulates close to the embedded Si NC's and at the Si/SiO_2 interface to form Si_3N_4 traps. These traps mask the NC related charging and discharging characteristics. In order to get rid of all these effects, the Ar gas was used for all experiments. Parasitic effects resulting from high temperature annealing of oxides in Ar at low partial pressure of oxygen are reported and discussed in chapter 9.

Device fabrication

Metal-oxide-semiconductor (MOS) capacitor devices were prepared for the electrical characterization of the NC containing gate oxides. Therefore, a 300 nm Al layer is sputtered on the front side of each chip and patterned lithographically to square and circular dots of different sizes. With a resist on top covering the Al layer, the thermal oxide from the back side was removed. After the lithography step 300 nm Al was also deposited on the back side to perform an ohmic back side contact. Subsequently, a 400°C furnace annealing was carried out for 20 nm in N_2. Sputter deposition causes plasma related defects in the oxide, especially the creation of dangling bonds at the Si/SiO_2 interface. The forming gas anneal is useful to passivate these defects supplying hydrogen. Usually this anneal is performed with a gas mixture of N_2 with 10 % H_2, but due to the presence of residual humidity in the furnace quartz tube a simple N_2 anneal is as effective as the gas mixture. No difference was obtained for the used equipment.

3 Methods of structural and compositional analysis

3.1 Imaging of Si and Ge NC's embedded in SiO_2 (TEM)

Aiming at the imaging of nanostructures the transmission electron microscopy (TEM) is the method of choice [228, 229]. Bright-field (using only the central direct electron beam) and dark-field (using a specific diffracted beam) are the primary imaging modes which can be both applied for high-resolution imaging. A conventional TEM operates without scanning the electron beam like in optical microscopy while scanning transmission microscopy (STEM) is based on a scanning beam similar to scanning electron microscopy (SEM). The image contrast - namely the mass (or Z-), diffraction, or phase contrast - depends on scattering and diffraction of electrons crossing the sample (usually of 20 to 150 nm thickness). Using auxiliary detectors a TEM provides also analytical techniques including energy dispersive x-ray spectrocopy (EDX) and electron energy loss spectroscopy (EELS) enabling the identification of elements, elemental maps and linescans.

Concerning the detection of Ge and Si nanocrystals or non-crystalline nanoparticles embedded in a SiO_2 matrix, the analysis of Ge NC's (or of particles consisting other heavy elements) benefits from a good Z-contrast with respect to the SiO_2 host material. There, a very powerful method is to collect the incoherently scattered electrons in STEM using a high-angle annular dark-field (HAADF) detector [228, 230]. As predicted by the Rutherford scattering equation with the differential scattering cross section of

$$\frac{d\sigma(\theta)}{d\Omega} = \frac{e^4 Z^2}{(16\pi\varepsilon_0)^2 E_0^2 sin^4\frac{\theta}{2}} \tag{3.1}$$

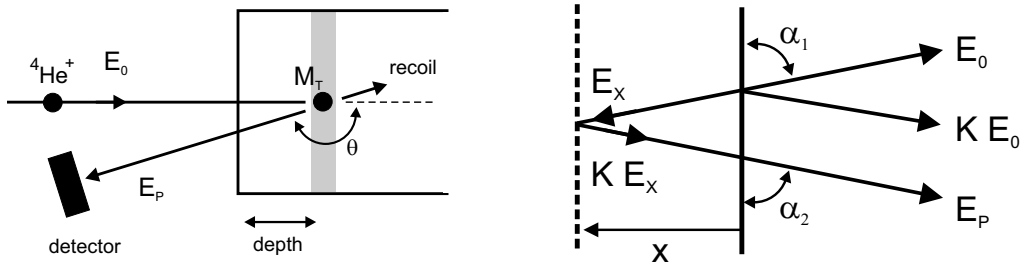
the intensity of the scattered electrons goes with the square of the atomic number (Z^2) for a sufficiently wide angular range, i.e. the contrast is improved for larger scattering angles (σ is the scattering cross section, ε_0 is the dielectric constant, Ω and θ are the solid and the scattering angle, respectively, with the incident beam energy E_0 and the atomic number Z of the scattering nucleus). But due to the small difference of atomic number and density between Si and SiO_2, it is very difficult to detect amorphous Si nanoparticles embedded in SiO_2, for instance [231]. Crystalline Si particles gain a contrast from the diffraction of electrons at their atomic planes (provided that a minimum number of planes assures sufficient periodicity), but only in the case if the planes of the NC's are almost parallel to the incident e-beam. As the NC's embedded in an amorphous matrix (like in SiO_2) are randomly oriented, the probability to detect one of these NC's by "fringes" (lattice plane imaging in high resolution TEM) is rather low. Additionally, the weak signal from

very small and rare NC's may disappear depending on the specimen thickness as the electrons are randomly scattered passing afterwards the amorphous oxide. Much more Si nanocrystals can be observed in low magnification in the dark-field mode scanning a larger sample area, but again only those which have the right plane orientation [53, 111]. For the detection of fringes a bulk-like crystal structure (diamond lattice) of the Si NC's is needed, but there is still an ongoing debate about the minimum particle size at which the Si clusters adopt this lattice configuration [211]: Si agglomerates of a few tens of Si atoms are discussed to have a prolate structure which consists of stacked Si_6-Si_{11} subunits [211]. The structural transition to a bulk diamond structure is supposed to be in the range of 300 - 500 atoms, which corresponds to a 2.3 - 2.7 nm small spherical Si NC's [214]. In fact, in TEM studies it was reported that the crystalline contrast disappears for Si particles below or equal 2 nm in size [213, 232]. This observation was also attributed to the size-dependent melting point of nanoparticles [211, 212] (see also chapter 2.8). Following this argumentation an extrapolation of related data yields that, e.g., silicon or gold nanoparticles with a size smaller than 2 nm should be no more solid even at room temperature [213, 215].

However, an option to visualize a high amount of small Si nanoparticles or -crystals in the oxide with reliable size and density information is to utilize the low-energy-loss domain around the Si plasmon energy loss peak in EELS measurements. There, energy filtered TEM (EFTEM) is used instead of conventional bright field TEM [26, 233, 234] for direct imaging where the contribution of the oxide matrix is minimized. The EFTEM gives an energy selected bright field image from those electrons, which are inelastically scattered at Si "bulk" plasmons crossing the specimen. Due the energy difference of the energy loss signal due to interaction with Si plasmons (16.7 eV) to the SiO_2 bulk related plasmon signal (22.5 eV) - the filtering energy window is typically 4 eV - Si dots are more clearly distinguishable from the surrounding oxide (resolution of the energy filter is typically about 0.8 eV). Recently, a reconstruction of the 3-dimensional shape of embedded Si nanoparticles succeeded by the so called "plasmon tomography" [235]. The 3D imaging reveals that some of the Si NC's, with a seemingly spherical shape in 2-dimensional cross-section TEM, have actually a much more complex and irregular, sometimes vermicular, morphology.

In general, the electron microscopy has to be performed with care, as due to inelastic scattering of the transmitted electrons the examined specimen heats up during the measurement [229]. Phonons are generated in the solid sample by the incident electrons. Additionally oxygen atoms from the oxide get displaced and released to the ambience. As a result nanocrystals can be also formed simply by electron beam exposure [236].

An alternative method is time-of-flight secondary ion mass spectrometry (ToF-SIMS) to proof the existence of, e.g. Si agglomerates in SiO_2 [141, 237]. The detection of Si_n^- clusters consisting of typically $n = 5$ or 6 Si atoms sputtered from the sample can be used as a fingerprint for the presence of Si NC's in SiO_2. An indirect proof of tiny Si NC's was also achieved using diffusing Ge as tracer atoms to decorate these Si precipitates [150].



(a) (b)

Figure 3.1: (a) Backscattering geometry for the incident He ion beam, the target sample and detector position for RBS measurements. (b) He ion energies before (E_0) and after interaction with surface atoms ($E_P = K\,E_0$) and with those located in oxide depth x (E_P) [238].

3.2 Rutherford backscattering spectrometry (RBS)

In Rutherford backscattering spectrometry (RBS) the sample of interest is irradiated with light ions (preferably $^4He^+$) with typical energy of 1 - 3 MeV analyzing the energy of the backscattered He ions [see Fig. 3.1(a)]. This nondestructive method delivers quantitative information of the mass, areal density and depth distribution of elements in the target without any need of calibrated standards. Using RBS under channelling conditions also information about the crystallinity of the substrate can be achieved. The kinematic factor K $(0 < K < 1)$ describes the ratio of the incident ion energy E_0 (with mass M_0) to that of the backscattered ion E_P after an elastic collision event with a surface target atom, for instance, of mass M_T with a backscattering angle of θ.

$$K = \frac{E_P}{E_0} = \frac{{M_0}^2}{(M_0 + M_T)^2}\left[cos\,\theta + \left(\sqrt{\frac{{M_T}^2}{{M_0}^2} - sin^2\,\theta}\right)\right]^2 \tag{3.2}$$

K simplifies to

$$K = \left(\frac{M_T - M_0}{M_0 + M_T}\right)^2 \tag{3.3}$$

assuming an ideal backscattering angle of $\theta = 180°$. The backscattering yield (total number of detected ions or counts) $A = \sigma\Omega N_S\,Q$ is a function of the average scattering cross section

$$\sigma = \frac{1}{\Omega}\int\left(\frac{d\sigma}{d\Omega}\right)d\Omega\,, \tag{3.4}$$

where N_S (in atoms/ cm^2) is the sample areal density, and Q the total number of incident ions. Ω is the detector solid angle in steradian [effective detector area / (detector to

sample distance)^2]. The differential scattering cross section is given by

$$\frac{d\sigma}{d\Omega} = \left(\frac{q^2 Z_0 Z_T}{2E_0 sin^2\,\theta}\right)^2 \frac{\left[\sqrt{1-(\frac{M_0}{M_T}\,sin\,\theta)^2}+cos\,\theta\right]^2}{\sqrt{1-(\frac{M_0}{M_T}\,sin\,\theta)^2}} \tag{3.5}$$

with the atomic number Z_0 and Z_T of the incident ion and the detected element in the target, respectively. Thus, RBS is most sensitive for heavy elements (high Z) embedded in a light matrix (low Z) as, e.g., for Au or Ge in SiO_2. This method is not suitable for the analysis of light elements with a mass close to helium ($K \approx 0$); for light elements the elastic recoil detection analysis (ERDA) should be used which is not applied in this thesis. If the impurity atoms in SiO_2 (e.g., Ge) are located close to the oxide surface, a Ge depth profile in SiO_2 can be obtained from the energy loss ΔE data.

$$\Delta E = E_0 K_{Ge} - E_P(d) = \Delta E_{in} K_{Ge} + \Delta E_{out} = [S_0]d \tag{3.6}$$

$E_P(d) = (E_0 - \Delta E_{in})K_{Ge} - \Delta E_{out}$ is the detected energy of the backscattered He atom coming from substrate depth d. The energy loss by electronic stopping of an incident He ion passing the oxide before and after the interaction with the scattering Ge atom is considered in ΔE_{in} and ΔE_{out}, respectively [see Fig. 3.1(b)]. This is subsumed in $[S_0]$, the depth dependent backscattering energy loss factor. Usually, the measurements shown in this thesis were obtained using 1.7 MeV He^+ ions at a total charge of 40 μC and a backscattering angle of $\theta = 170°$. The depth resolution was improved from typically 10 nm to about 2 nm working in grazing incidence with an angle of 70° perpendicular to the surface normal. As the stopping power dE/dx, the kinematic factor K and the differential capture cross section $d\sigma/d\Omega$ are well known or well defined parameter, the data extraction succeeds without the need of calibrated standards. For further details to this method see Refs. [238, 239, 240] and also [241].

3.3 Hydrogen profiling using nuclear reaction analysis (NRA)

For the detection of light elements (from hydrogen to fluorine) and their depth distribution in some cases a nuclear resonance reaction can be utilized. Accelerated ions with a specific energy interact with target nuclei under release of γ-rays and/or secondary particles. Here, the hydrogen content and its depth distribution in SiO_2 is obtained by the resonance reaction ^{1}H(^{15}N, $\alpha\gamma$)^{12}C using the narrow resonance at the ^{15}N energy of $E_r = 6.385$ MeV.

$$^1\mathrm{H} + {}^{15}\mathrm{N} \longrightarrow {}^{16}\mathrm{O}^\star \longrightarrow {}^{12}\mathrm{C} + {}^4\mathrm{He} + \gamma\,(4.43\,\mathrm{MeV}) \quad . \tag{3.7}$$

If a ^{15}N atom with energy E_r strikes a H atom in SiO_2, a nuclear reaction may happen, where a highly excited ^{16}O* compound nucleus is formed which decays to ^{12}C under emission of an α-particle and a gamma quantum having the characteristic energy of

$E_\gamma = 4.43$ MeV. The γ radiation is counted to obtain the hydrogen content in the target, whereas the γ-yield is proportional to the hydrogen amount. A plastic foil with known hydrogen content is used for calibration (see Ref. [242] for details of data evaluation). For depth profiling the energy E_0 of the incident $^{15}N^+$ ions is continuously increased ($E_0 > E_r$) which shifts the specific resonance energy E_r needed for the nuclear reaction with H from the surface to a depth d inside the oxide. From the known stopping power value of ^{15}N in SiO_2 (dE/dx) a depth scale is calculated with

$$d \;=\; (E_0 - E_r)\left(\frac{dE}{dx}\right)^{-1} \quad . \tag{3.8}$$

Using NRA the resolution limit of hydrogen in SiO_2 is about 0.02 at.%. For the presented investigations the oxide is irradiated by $^{15}N^{2+}$ ions under an incidence angle of 15° with respect to the sample surface to improve the depth resolution to about 2 nm. For details to the NRA method see also Ref. [239].

4 Electrical modeling and characterization of nanocrystal containing gate oxides

As shown by De Salvo *et al.* [73] the dynamic charging and discharging behavior of NC containing gate oxides follows a floating-gate-like [10] behavior (see Fig. 4.1 and also chapter 1.2). In this description R_{nc}, depending on the NC density and size [Eq. (1.5)], defines the portion of the floating gate which is in the projection covered by NC's. The charge exchange between the Si substrate or gate electrode and the NC's occurs via direct or Fowler-Nordheim (FN) tunneling of electrons (or holes) across the tunneling or control oxide [d_{tox} and d_{cox} in Fig. 4.1(b)], respectively [73]. A detailed analysis reveals [73] that Shockley-Read-Hall processes, describing the charge capture and emission at or from traps, are not suitable to describe NC containing memory devices in contrary to silicon nitride containing ones (SONOS). The thermally activated charge capture or emission from deep trap level states at the Si NC/SiO_2 interface does not dominate the charge exchange between the Si NC's and the Si channel [72, 73]. As already the tunneling current characteristics change with device temperature, a temperature dependent retention behavior has not to be necessarily connected to storage at deep traps [12, 73, 243]. In case that the charge storage is negligible, the leakage current through NC containing gates oxides is explained by elastic tunneling of electrons [18].

In the past decade the electrical modeling of NC containing gate oxides has been a very rare subject in the research area, especially concerning their charge transfer characteristics (gate oxide leakage currents): Recently, a Si NC memory cell was electrically modeled (and measured) with respect to its programming and erase dynamics [244]. The device

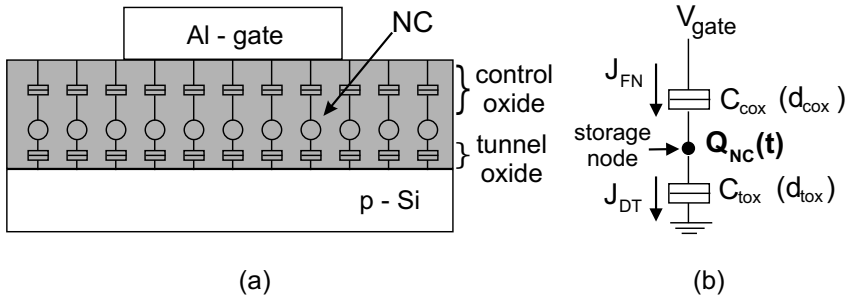


Figure 4.1: (a) Structure model of a NC containing metal-oxide-silicon capacitor device. (b) Equivalent circuit for one NC as a floating gate storage node (for details see Ref. [75]).

consists of a layer of $N_{nc} = 5 \times 10^{11}\,\mathrm{cm}^{-2}$ NC's with 6 nm diameter sandwiched between a 2.8 nm tunneling- and a 6 nm control oxide. There, a one-dimensional code was used to calculate internal potential profiles solving the Schrödinger-Poisson equations as a function of the applied gate voltage. It should be mentioned that the computed current-voltage characteristics are in considerable agreement to those presented in this thesis (chapter 8). But, capacitive coupling among the NC's as well as quantum confinement effects were not taken into account. A description of a quantum dot memory device is given in Ref. [245] using the transition-Hamiltonian to evaluate the tunneling rates of electrons. In this publication only basic capacitance-voltage and source-drain current characteristics are presented. Rana *et al.* [246] consider Coulomb charging effects in their calculations but only for a memory device with a single quantum dot with limited comparability to multidot memory devices.

Si nanodot memory simulations address mainly the programming window distributions related to typical technological dot size or dot number fluctuations with respect to the chemical vapor deposition technique [19]. Effects of nonuniform charge distribution on the memory device characteristics were discussed [247] as well as the programming window dependence on the channel width [248], or the intrinsic reliability limits of floating-gate-like devices in the decananometer range scales [249]. But in the floating-gate-like approach for a NC based memory device, the NC size and density - represented by the projected coverage ratio R_{nc} in Eq. (1.5) - are only linear factors in the charging of the embedded NC's [18, 73].

$$\frac{dQ_{fg}}{dt} = R_{nc}(J_{in} - J_{out}) \tag{4.1}$$

The charge amount stored at the NC's Q_{fg} changes due to charging and discharging currents J_{in} and J_{out}, but proportional to R_{nc}. As these currents depend exponentially on the voltage drop and the electrical fields across the tunneling or control oxides [see $E_{ox} = V_{ox}/d_{ox}$ in Eq.(4.5)], a variation in the tunneling oxide thickness d_{tox} is much more significant for the programming characteristics than the NC size or spatial distribution in plane. Usually this topic is disregarded arguing that in CVD processing the NC's are deposited on a homogeneously flat thermally grown tunneling oxide. But, as shown by Puglisi *et al.* [233] during post-deposition annealing treatments ripening of the dots takes place (growing and shrinking of NC's) which of course changes the individual tunneling distances of the NC's to the Si substrate.

In this thesis, a floating-gate-like model has been developed to describe the transient charging behavior of NC containing gate oxides (see chapter 6). The electrical model is based on general equations for nonvolatile devices, e.g., for the floating gate potential V_{fg} and charge density Q_{fg} in Eq. (1.1) and (1.2), respectively. The charging and discharging of the NC's follows the formulas of direct and Fowler-Nordheim tunneling derived from a parabolic dispersion relation in the Wenzel-Kramers-Brillouin (WKB) approximation (see equations in chapter 4.1) [250, 251, 252]. The role of quantum confinement and Coulomb blockade effects are discussed defining a range of NC densities and sizes in the oxide, where this model is applicable. In chapter 7 it will be shown that this model is suitable to derive the distribution of tunneling oxides thicknesses for the individual NC's using simple programming characteristics. Changes in the tunneling oxide thickness due

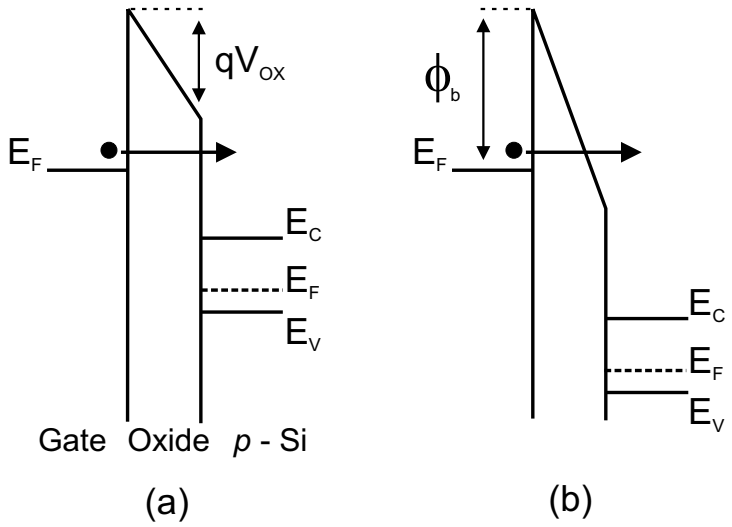


Figure 4.2: Energy-band diagram illustrating (a) the direct electron tunneling through a trapezoidal barrier ($qV_{ox} < \phi_b$) in comparison to (b) the Fowler-Nordheim tunneling through a triangular barrier ($qV_{ox} \geq \phi_b$).

to thermal annealing are shown to be in agreement to the theory of Ostwald ripening. The dissolution of small NC's adjacent to the Si substrate corresponds to a local tunneling oxide growth. The transient electrical model as introduced in chapter 6 and 7 is valid for all NC based memory devices however the NC's are synthesized. The ion beam synthesis yields a spatially statistically distribution of NC's which reveals the role of a tunneling oxide thickness variance for the NC based memory performance. This underlines the significance of the present study.

4.1 Fowler-Nordheim and direct tunneling

Fowler-Nordheim (F-N) tunneling [253] is the most-established charge conduction mechanism through thin silica films. Widely used formulas have been evidenced by Lenzlinger and Snow [254] and later by Weinberg *et al.* [250, 255]. The F-N current [Eq. (4.2)] is mainly depending on the tunneling barrier height ϕ_b (in eV), the oxide electrical field E_{ox} (in MV / cm), and the effective masses of charge carriers in the oxide m_{ox}. $m_{ox} = 0.5\, m_0$ is valid for all gate electrode materials with respect to SiO_2 [250] (m_0 is the free electron mass).

$$J_{FN} = \frac{q^3 m_{si}}{8\pi h m_{ox} \phi_b} E_{ox}^2 exp\left(-\frac{8\pi\sqrt{2m_{ox}}}{3hqE_{ox}}\phi_b^{3/2}\right) \tag{4.2}$$

h is Planck's constant, q the elementary charge, and m_{si} the effective electron (or hole) mass in Si. For very thin oxides ($d_{ox} < 4.5\,\text{nm}$) direct tunneling of electrons or holes dominates at low oxide electrical fields (see Figs. 4.2 and 4.3). The widely used analytical

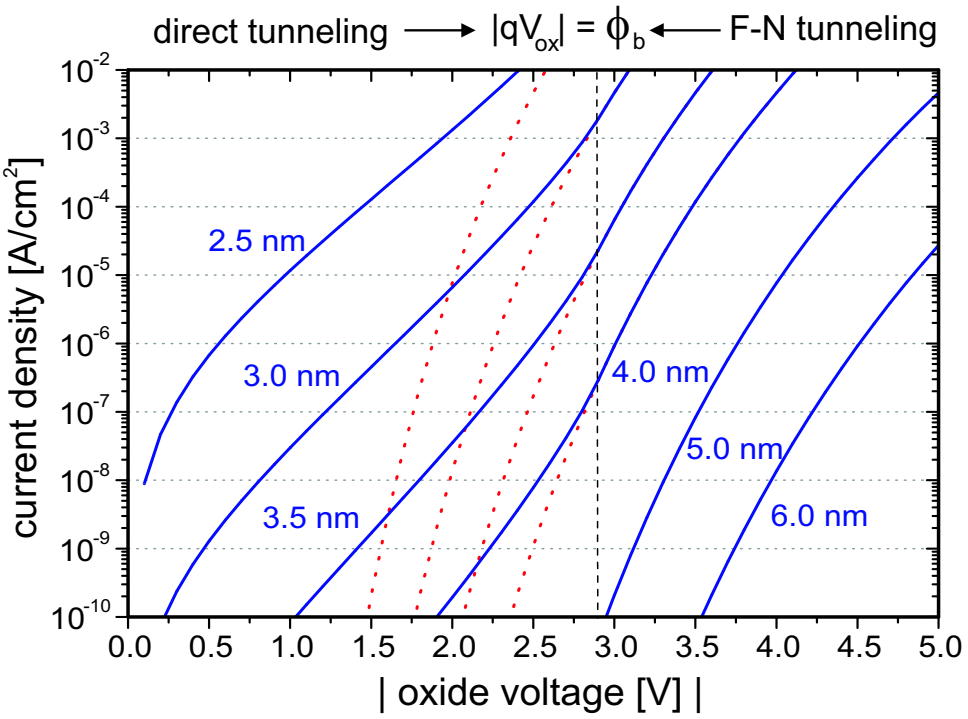


Figure 4.3: Current-voltage characteristics calculated after Eq. (4.5) for direct and F-N electron tunneling for oxides of 2.5 - 6.0 nm thickness. As parameter $\phi_b = 2.9\,\mathrm{eV}$, $m_{ox} = 0.5\,\mathrm{m_0}$, and $\mathrm{m}_{si} \approx \mathrm{m_0}$ are used for electron injection from an n-type Si substrate in accumulation, for instance. The F-N tunneling parts of the characteristics at low electrical oxide fields are indicated by red dotted lines. They dominate the total tunneling current for $|qV_{ox}| \approx \phi_b$.

formula derived by Schuegraf *et al.* [251, 256, 257]

$$J_{DT} = \frac{q^3}{8\pi h \phi_b}\left(\frac{\phi_b}{V_{ox}}\right)\left(\frac{2\phi_b}{V_{ox}-1}E_{ox}^2\right) exp\left(-\frac{8\pi\sqrt{2m_{ox}}}{3hq}\,\frac{\phi_b^{3/2}-(\phi_b-qV_{ox})^{3/2}}{E_{ox}}\right) \qquad (4.3)$$

is not suitable for oxide voltages $V_{ox} < 1\,\mathrm{V}$, as the current in Eq. (4.3) does not approach zero for $V_{ox} \to 0$ V. Alternatively, a semi-empirical equation should be used to calculate the direct tunneling current as done by Lee *et al.* [252], or the simplified equation of Schuegraf *et al.* [251]:

$$J_{DT} = \frac{q^3 m_{si}}{8\pi h m_{ox}\phi_b}E_{ox}^2 exp\left(-\frac{8\pi\sqrt{2m_{ox}}}{3hq}\,\frac{\phi_b^{3/2}-(\phi_b-qV_{ox})^{3/2}}{E_{ox}}\right) \quad . \qquad (4.4)$$

The latter equation provides a good fit to experimental data for a tunneling barrier height ϕ_b of 2.9 and 4.5 eV and an effective mass in the oxide m_{ox} of $0.42\,m_0$ and $0.32\,m_0$ for electrons and holes, respectively, as shown in chapters 6 and 8. A common prefactor

for direct and F-N tunneling in Eqs. (4.2) and (4.4) enables a simple unification of both tunneling mechanisms in a single formula.

$$J_{DT-FN} = AE_{ox}^2 exp\left(-B\,\frac{\phi_b^{3/2} - (\phi_b - qV_{ox})^{3/2} \times H(\phi_b - qV_{ox})}{E_{ox}}\right) \tag{4.5}$$

$H(\Gamma)$ is the Heaviside-function with $H(\Gamma) = 0$ for $\Gamma \leq 0$ and $H(\Gamma) = 1$ for $\Gamma > 0$ with $\Gamma = (\phi_b - qV_{ox})$. The coefficients A and B yield

$$A = \frac{q^3 m_{si}}{8\pi h m_{ox} \phi_b} \quad \text{and} \quad B = \frac{8\pi\sqrt{2m_{ox}}}{3hq} \quad . \tag{4.6}$$

Typical current-voltage characteristics are calculated after Eq. (4.5) and shown in Fig. 4.3 for a single barrier height ϕ_b and charge carrier effective mass m_{ox} for both tunneling processes.

4.2 Electrical properties of ion implanted gate oxides

A trap-assisted charge transport model neglecting NC's in the oxide

For ion implanted oxides (mainly using Si ions) enhanced gate oxide leakage currents were obtained which increase at higher ion fluences [36, 151, 152, 153, 157, 258]. In comparison to virgin gate oxides, after ion implantation and annealing the current-voltage characteristics behave similar to a Fowler-Nordheim (F-N) characteristic, but shifted toward lower gate voltages and possess a weaker slope in the high field region. Neglecting any charging of the oxide, at first a trap-assisted charge conduction model was proposed in the literature to describe such a behavior [159, 259]. Traps are assumed to be generated by the ion implantation in the oxide mainly close to the injecting electrode/SiO_2 interfaces. Using the common F-N tunneling formula [Eq. (4.2)] this effect is included considering an effective barrier lowering for the injected tunneling electrons. In a more qualitative study by Kameda *et al.* [258] the charge transport was assigned to be trap-assisted in combination with F-N tunneling of electrons, whereas traps in the oxide nearby the electrodes are filled or emptied by direct electron and hole tunneling. But, already in the early 1980s a significant charging was found by DiMaria *et al.* [260] and Kalnitsky *et al.* [261] for Si-rich and also for Si implanted oxide layers, respectively. There, they discussed for the first time the applicability of such structures for memory devices. Additionally, Kalnitsky *et al.* [262] developed the so far unique charge transport model (except the present work) for Si ion implanted thermally grown SiO_2 layers. A significant redistribution of the implanted Si atoms and so the formation of Si NC's in the oxide was excluded for annealing treatments below 1300°C [151, 263] due to a very low diffusivity of Si in SiO_2 of $D = 328$ exp (- 6 eV/ kT) cm^2/s based on the findings of Brebec *et al.* [122] (see also chapter 2.2). Thus, a trap distribution in the oxide was considered which follows the initial Si ion impurity profile in the oxide right after ion implantation. In general, electrode limited models (like F-N or direct tunneling) give more reliable results for the

charge conduction through ion implanted oxides than the bulk limited charge hopping transport (Poole-Frenkel [264]) [262, 265].

In several publications in the early 1990s the applicability of Si implanted gate oxides ($d_{ox} \leq 50$ nm) for memory devices was proved on MOSFETs [153, 154]. Significant shifts of the threshold voltage V_t at low gate oxide electrical fields (3 - 7 MV/cm) were obtained with programming pulse lengths in the range of milliseconds [153]. A data retention for more than 100 h was shown depending on the oxide thickness and the implantation parameters [154]. Such devices reveal a very good endurance which means that device holds for much more than 10^6 write/erase cycles (typically up to 10^9) [21, 153, 156]. But, without any evidence of NC formation, the charge transport and the memory effect were still regarded as trap-induced with traps generated by the Si ion implantation. In the mid 1990s Tiwari *et al.* [1] demonstrated that the charge storage is related to Si NC's present in the SiO_2 layer. They work as storage nodes regardless of the preparation technique - chemical vapor deposition or Ge/Si ion implantation [21]. Si, Ge, and also metal nanocrystals form even at much lower temperatures than considered in the work of Kalnitsky *et al.* [151, 263]. It is clear that since this time the existence of NC's has to be necessarily included in the modeling of charge storage or charge transfer characteristics discussing the memory behavior of nanocrystal containing memory devices. But just rare work has been published related to the the electrical modeling of nanocrystal containing gate oxides, especially for NC's prepared by ion beam synthesis in thin gate oxides.

Electrical properties of the Si/SiO_2 interface after ion implantation and annealing

A good quality of the Si/SiO_2 interface and of the underlying Si channel region are vital requirements of modern CMOS transistor device processing. Due to the broad profile of the implanted impurity ions in the gate oxide both areas are involved (see chapter 2.6). After the subsequent annealing the Si/SiO_2 interface and the Si bulk restores depending on the applied annealing conditions, i.e., the annealing temperature/time and the oxygen content in the annealing ambience. Thus, due to the significant dependence on the processing parameter, the reported data are often contradictory describing the electrical properties of the Si/SiO_2 interface. Hori *et al.* [153] found that the density of interface states D_{it} remains at midgap in the $10^{10}\,cm^{-2}/eV$ range after Si implantation and annealing (see also Ref. [266]). A correlation between the amount of Si excess at the Si/SiO_2 interface (caused by the Si^+ implantation) to the final trap density was found by others [262]. A clear Si-fluence dependence on the threshold voltage, the electron mobility in the Si channel, and the subthreshold swing was found closely related with D_{it} [267] which was denied by others [262]. Considering a memory device application quite acceptable data for the subthreshold swing were obtained (in the range of 84 mV/dec - 115 mV/dec) for different degrees of interface damaging [148, 266, 268]. As confirmed by several investigations, annealing in diluted oxygen improves the quality of the oxide and also of the Si/SiO_2 interface [139, 152, 262]. Apparently, the oxidation of excess Si is helpful for a better recovery of the damaged SiO_2 network. In this thesis a very dynamic charging and discharging behavior of the Ge NC containing gate oxides was found which modifies the shape of the capacitance-voltage (C-V) characteristics even for small gate voltage

sweeps. Thus, a detailed analysis of the electrical properties of the Si/SiO_2 interface after Ge and Si NC ion beam synthesis is not shown because reliable data for the interface state density (D_{it}) were hardly achievable (see chapter 6). Approximated by frequency dependent conductance - voltage measurements (conductance method [241, 269]) D_{it} data were obtained to be at midgap in the range of $1\text{-}10\times10^{10}\,\mathrm{cm}^{-2}/\mathrm{eV}$ for the Si implanted samples and slightly above $1\times10^{11}\,\mathrm{cm}^{-2}/\mathrm{eV}$ for the Ge implanted samples. But both vary with the individual implantation and annealing parameters. Finally, it should be mentioned that the measured oxide capacitance increases with increasing ion implantation fluence as a parasitic effect of ion implantation. The additional off-stoichiometric amount of Si in SiO_2 changes considerably the total dielectric constant of the oxide layer ($\varepsilon_{SiO2} = 3.9\,\varepsilon_0$, $\varepsilon_{Si} = 11.8\,\varepsilon_0$) [262, 270, 271].

4.3 Tracing the NC charging and discharging behavior on MOS capacitors

On metal-oxide-semiconductor (MOS) capacitor devices the charging and discharging behavior of the embedded NC's is traced by means of capacitance-voltage (C-V) measurements. For transistor devices the amount of stored charges in the NC's Q_{nc} (in units of C/cm^2) is obtained from the threshold voltage shift ΔV_t after Eq. (1.4) sensing the source-drain current. Using a similar expression for MOS capacitor devices the same data is achieved from the shift of the flatband voltage V_{fb} with known location of the stored charges in the gate oxide (e.g., in the center of the NC's).

$$\Delta V_{fb}(t) = V_{fb}(t) - V_{fb}(t_0) = -\,Q_{nc}(t)\left(\frac{d_{cox}}{\varepsilon_{ox}} + \frac{1}{2}\frac{d_{nc}}{\varepsilon_{nc}}\right) \tag{4.7}$$

$V_{fb}(t_0)$ is the flat-band voltage for the initial uncharged device (see also Fig. 1.4). Details for the C-V measurement technique and data analysis are extensively discussed by Nicollian and Brews in Ref. [269] and also in Refs. [16] and [241].

Sometimes the memory effect of MOS capacitors is only characterized by C-V hysteresis measurements with inherently insufficiently defined programming, erase and readout conditions. In recent publications two serious ways are discussed to study the discharging process of NC containing gate oxides on capacitor devices [272], the constant capacitance method (CCM) [72] and the constant bias method (CBM) [272]. In the first case (CCM), after the initial charging pulse, a variable gate voltage is applied to follow currently the transient discharging at a fixed capacitance value, e.g., the flat-band capacitance C_{fb}. The recorded voltage data are then equal to the flat-band voltage as a function of time $V_{fb}(t)$. In this case usually a very convenient charge decay characteristic is achieved. With Gauss' law $\varepsilon_{si}E_{si} = \varepsilon_{ox}E_{ox}$ - to fulfil the Si substrate/SiO_2 boundary condition (neglecting interface trapped charges) - the electrical field in the tunneling oxide E_{ox} is kept zero at a substrate surface potential of $\psi_s = 0\,\mathrm{V}$ (flat-band condition!). This is exactly the case if the measured capacitance data is kept constant at C_{fb}. E_{si} and E_{ox} or ε_{si} and ε_{ox} are the electrical fields and dielectric constants in the Si substrate and the gate oxide,

respectively. In this method the major charge loss mechanism across the tunneling oxide - the direct tunneling from the NC's to the Si substrate - is clearly affected or actually inhibited. There, the applied voltage drops mainly across the control oxide forcing a parasitic charge exchange with the gate electrode for high flat-band voltage shifts. In the constant bias method (CBM) an artificial bias (non-zero) is applied during data storage in contrary to the case of a real memory device [272]. Capacitance data are recorded as a function of waiting time. The retention data are calculated using the C-V data of a virgin device as a reference. Using the linear part of the C-V characteristics around C_{fb} with the highest sensitivity to V_{fb} changes, this method is only suitable for insufficiently small flatband voltage shift amplitudes. Large V_{fb} shifts can not be obtained by a single gate voltage bias. Additionally, the shape of a C-V characteristic is strongly depending on process parameters (e.g., the gate oxide thickness, the substrate doping, D_{it}, etc. [269]). Thus, with a variable voltage range for data acquisition this method has a limited reproducibility and comparability. As a consequence, both the CCM and the CBM were found not to be useful for the structures focussed in this thesis.

Very dynamic memory effects as reported for ultra-thin (≤ 2 nm) tunneling oxides [273, 274] challenge special measurement routines to trace the short-time discharging processes (< 1 s) [275]. In this thesis the measurement of a reference (uncharged) C-V characteristic is necessary to obtain the initial flat-band voltage value $V_{fb}(t_0)$. After the programming pulse short (3 - 300 ms) read pulses are applied with increasing storage time to obtain capacitance data C_{meas} tracing the discharging of the embedded NC's (see chapter 6). In detail, in each read period a series of two or three quickly repeated pulses are applied to find the actual flat-band voltage at $C_{meas} \approx C_{fb}$. The last voltage datum is the starting point for the next readout interval. Between the read pulses no artificial bias is applied, i.e., $V_g = 0$ V for a limited impact of storage data acquisition. Thus, a definite condition is established presumably similar to memory device "off" state. With a shortened substrate and gate electrode ($V_g = 0$ V) the voltage drop over the tunneling and control oxide is directly forced by the amount of charges stored at the NC's. In comparison to the others this method represents a worst case scenario. The minimum read pulse duration (3 ms) is limited by the capacitance data acquisition time of the Keithley 590 CV analyzer.

5 Utilizing a Ge redistribution in the oxide during annealing to prepare nanodot memory devices

Elemental redistribution and Ge loss during ion-beam synthesis of Ge nanocrystals in SiO_2 films

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The elemental redistribution and Ge loss in low-energy Ge^+ implanted SiO_2 films during wet-chemical cleaning and annealing procedures are investigated. Two effects of major importance for Ge nanocrystal formation have been found. Moisture components (H_2O vapor, H^+, OH^-) penetrate into the damaged oxide during storage, cleaning or annealing procedure and lead to an additional hydrogen and oxygen content with a diffusion-like profile in the near-surface oxide. Furthermore, atomic collisions during Ge implantation result in an oxygen excess (with respect to SiO_2 stoichiometry) close to the Ge profile. The local net ratio of Ge and excess oxygen determines, whether the implanted Ge is incorporated into the SiO_2 network as spatially fixed GeO_2, oxidizes to mobile GeO or remains as elemental Ge forming nanocrystals. Apart from very shallow profiles, where a drastic Ge loss is observed simply by cleaning in chemical solutions containing H_2O_2, the main Ge loss occurs during annealing. The highly mobile GeO is identified to be responsible for both, Ge redistribution or even loss, if diffusing GeO meets the SiO_2 surface and emanates into the annealing ambient. Annealing in Ar/H_2 mixtures at $\leq 900°C$ reduces the Ge loss due to the reduction of Ge oxides. The enhanced Ge mobility (as GeO) is described as an oxygen vacancy assisted mechanism which also explains the influence of the Si/SiO_2 interface on the Ge diffusivity. Finally, the consequences of Ge redistribution and loss for Ge nanocrystal memory device fabrication are discussed.

PACS numbers: 68.55.Ln, 66.30.h, 61.46.Hk

I. INTRODUCTION

Group-IV (in particular Si or Ge) nanocrystals (NC's) embedded in thin SiO_2 gate dielectrics are of fundamental interest for integrated multidot memory devices.[1,2] It has been shown that such NC containing thin gate oxides ($d_{ox} \leq 30\,nm$) exhibit charge storage properties with non-volatile (Si NC's) or DRAM-like (Ge NC's) memory behavior.[3–7] The NC's are preferably fabricated by deposition techniques (sputtering, chemical vapor deposition, aerosol spraying) or ion beam synthesis (IBS).[8] The versatile technology of IBS offers the possibility to generate small clusters (size $< 4\,nm$) of different elements (Si, Ge, Au, Sn, Co, etc.) with a high density ($>10^{12}\,cm^{-2}$) in SiO_2 simply by the variation of the ion species, energy, and fluence of ion implantation.

The IBS process requires an annealing step after ion implantation to recover the damaged oxide and to stimulate the NC's growth. For Ge implanted SiO_2 films this heat treatment is usually associated with two effects of considerable influence on NC's formation: (i) a change of the Gaussian-like implantation profile toward a multimodal Ge distribution, and (ii) a partial loss of the implanted Ge amount. Both effects are much pronounced in thin gate oxides when the implanted Ge is located very close to the surface. The redistribution effect has been advantageously used for the formation of a self-organized δ layer of Ge NC's in vicinity to the Si/SiO_2-interface[3,9–12] which is a desired configuration to achieve multidot memories with low programming voltages and/or times.

For thick SiO_2 films ($d_{ox} > 100\,nm$) the influence of implantation and annealing conditions on the Ge redistribution has been studied by numerous investigations,[10,13–19] however the detailed mechanism remains under discussion. It is widely accepted that both, redistribution and loss are strongly influenced by moisture contaminants (H_2O, OH, H_2) which penetrate the damaged oxide after ion implantation.[20] These species originate either from air humidity and wet cleaning chemicals ("intrinsic source") or from the residual moisture in the "inert" Ar or N_2 annealing ambient ("extrinsic source"). During annealing the excess oxygen and hydrogen may react with Ge leading to the formation of amorphous GeO_2 and mobile (volatile) compounds like GeH_4 or GeO. In detail, the effect of Ge oxidation during annealing was studied by Heinig *et al.*[15] and Borodin *et al.*[16] for 500 nm SiO_2 films. Their kinetic 3D lattice Monte-Carlo (KLMC) simulations consider the diffusion of two kinds of interacting impurities - dissolved Ge monomers and an oxidizing component (e.g. O_2, OH). The simulated Ge redistribution and the formation of near-surface GeO_2 are in good agreement with the experimental results obtained by x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). But, as the GeO_2 is spatially fixed, any Ge loss can not be explained by this model. The considerable loss ($\sim 50\%$) after a furnace annealing of Ge implanted SiO_2 films at $T = 1100°C$ in $Ar + 7\%\,H_2$ found by Markwitz *et al.*[14,21] was attributed to volatile GeH_4 or GeO but no experimental evidence has been reported.

In this paper the Ge redistribution and loss is studied for low-energy implanted SiO_2 films where the Ge is located in a very near-surface region ($\leq 20\,nm$). This is of

particular interest for the synthesis of Ge NC's in thin gate oxides being designed for memory devices. Besides the variation of the ion energy and fluence, experimental conditions were selected which allow the separation of effects from cleaning and annealing. Based on the experimental results a qualitative discussion of the mechanisms and chemical processes involved in the Ge redistribution and loss is given.

II. EXPERIMENT

A. Sample Processing

Low-energy implantations of $^{74}Ge^{+}$ ions ($E \leq 12\,\mathrm{keV}$) were carried out into $1\,\mu$m, 100 nm or 50 nm SiO_2 films thermally grown on Si(100) substrates. The implantation parameters are summarized in Table I. Different energies (1.5 - 12 keV) and two fluences [low/high fluence: LD / HD (labeling after the more technical terms 'low dose' and 'high dose')] were used to investigate the depth and concentration dependence on the Ge redistribution and loss. After ion implantation a common wet-chemical cleaning step in H_2O_2/H_2SO_4 (CP1) was performed (see Table II). A cleaning is necessary before annealing to remove possible contaminations from implantation handling. The influence of the different chemical components during the pre-anneal cleaning treatment was investigated separately for samples implanted with the lowest energy ($E = 1.5\,\mathrm{keV}$). Here, the cleaning sequence has been stepwise reduced as described in Table II.

Rapid thermal annealings (RTA) were carried out at temperatures between 600°C and 1050°C in different atmospheres for times between 30 s and 10 min. In most cases, the annealing was performed in an ultra-pure "inert" Ar ambient (purity 9.0 with respect to O_2, OH) by using an Aeronex gas purifier. For these conditions, the influence of the "extrinsic source" on the Ge redistribution can be neglected. For comparison, a few anneals were performed in gas mixtures of $Ar + 5\%\,O_2$ or $Ar + 5\%\,H_2$ to stimulate the impact of oxygen or hydrogen. Thus, the separation of effects related to the penetration of moisture before annealing or from the annealing ambient is possible. In a separate experiment, Si ions were implanted ($200\,\mathrm{keV} / 1\times10^{16}\,\mathrm{cm}^{-2}$) prior to Ge to study the influence of an additional deep oxide damage - where a higher amount of penetrated moisture in the oxide can be suggested - on the Ge loss and redistribution.

TABLE I: Implantation and annealing parameters. For different implantation energies the fluences were adjusted to ensure an uniform maximal Ge content of approximately 7 or 17 at.% for the LD or HD implants, respectively.

Series	SiO_2	Ion Implantation				Annealing
	d_{ox} (nm)	Ion	E (keV)	LD (cm^{-2})	HD (cm^{-2})	
A	1000	^{74}Ge	1.5	1.8×10^{15}	5.1×10^{15}	Ar (9.0)
			3	2.4×10^{15}	6.8×10^{15}	600-1050°C
			6	3.4×10^{15}	9.5×10^{15}	30 s / 10 min
			12	4.9×10^{15}	1.4×10^{16}	
B	100	^{74}Ge	12	-	1.8×10^{16}	Ar (9.0)/
	100	^{74}Ge	12	-	1.8×10^{16}	$Ar + 5\%\,O_2$ /
		^{28}Si	200	-	1.0×10^{16}	$Ar + 5\%\,H_2$
	50	^{74}Ge	12	-	1.8×10^{16}	900°C/
		^{28}Si	200	-	1.0×10^{16}	1000°C, 5 min

TABLE II: Process sequence and parameters of the wet-chemical H_2O_2/H_2SO_4 cleaning treatment (CP1) and the modified cleaning procedures (CP2 - CP4).

	Step 1	Step 2	Step 3	Step 4
Process sequence	Boiling H_2O_2/H_2SO_4	Ultrasonic Deionized H_2O	Ultrasonic Isopropanol (C_3H_8O)	Drying N_2 flow
	120°C	20°C	20°C	20°C
	10 min	10 min	1 min	
CP1	✓	✓	✓	✓
CP2 (step 1 without H_2O_2)		✓	✓	✓
CP3			✓	✓
CP4				✓

B. Analysis Techniques

The content and depth distribution of Ge in SiO_2 was traced by Rutherford backscattering spectrometry (RBS) using 1.2 MeV He ions at an scattering angle of 170°. To improve the depth resolution an incidence angle of typically 70° perpendicular to the surface normal was used. The penetration of hydrogen or hydrogen containing species (H_2O, OH^-, H^+) into the damaged SiO_2 after implantation and cleaning was detected by means of nuclear reaction analysis (NRA) using the resonance reaction

$$^{1}\mathrm{H} + {}^{15}\mathrm{N} \longrightarrow {}^{12}\mathrm{C} + {}^{4}_{2}\mathrm{He} + \gamma\,(4.43\,\mathrm{MeV}) \quad . \quad (1)$$

Details of this technique and the data evaluation are described elsewhere.[22] The chemical state of Ge was analyzed by XPS. The measurements were performed by a Microlab 310F (Fisions) spectrometer using a Mg x-ray tube ($E = 1254\,\mathrm{eV}$). The inelastic mean free path of photoelectrons in SiO_2 is $\leq 3.3\,\mathrm{nm}$[23] which determines the XPS information depth. Within this study the analysis is restricted to samples implanted with the lowest energy ($E = 1.5\,\mathrm{keV}$) to exclude any influence of the sputtering process during depth profiling on the chemical information.[24] The XPS spectra are calibrated in energy and intensity to the C 1s peak (285.0 eV) and the O 2s signal,

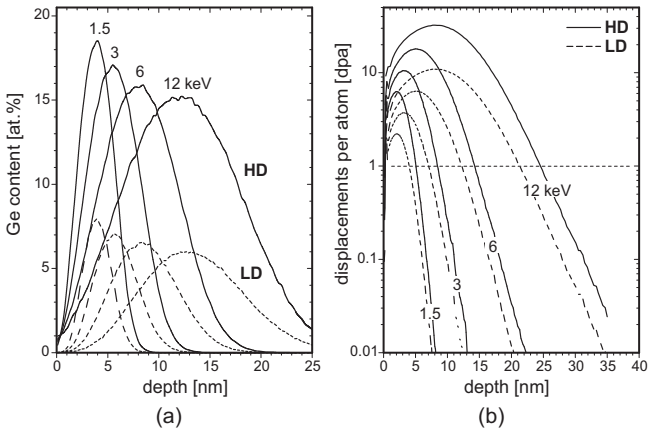


FIG. 1: (a) Ge profiles according to the implantation parameters of Table I, series A; (b) Corresponding damage distribution in terms of the dpa rate. The HD and LD profiles are plotted with closed and dashed lines, respectively.

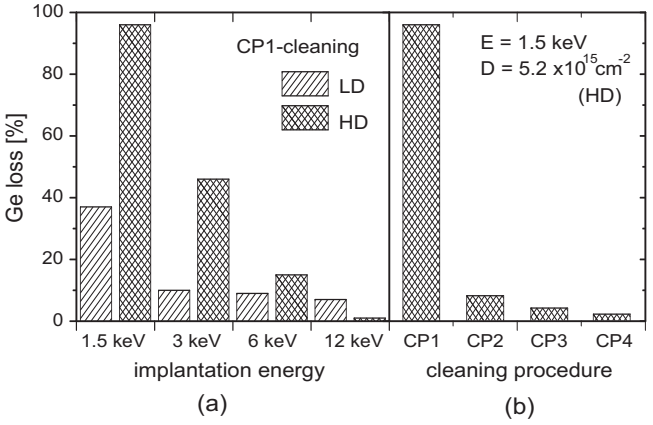


FIG. 2: Loss of Ge due to wet-chemical cleaning treatment obtained from RBS data (not shown) using the as-implanted sample as a reference. (a) Ge loss after a standard H_2O_2/H_2SO_4 cleaning procedure before the annealing treatment. (b) A stepwise investigation of the complete cleaning sequence isolates the H_2O_2 as the main component responsible for the Ge loss during cleaning.

respectively. The latter is dominated by oxygen from the SiO_2 network and is thus considered as a reference.

III. RESULTS AND DISCUSSION

Figure 1 shows the Ge implantation profiles and the corresponding damage distributions as calculated by TRIDYN[25] and SRIM,[26] respectively. Depending on the energy, the projected range R_p varies between 4 nm ($E = 1.5$ keV) and 13 nm ($E = 12$ keV). The slight decrease of the peak concentration with energy (compared to uniform 7 and 17 at.% for LD and HD, respectively, as estimated by SRIM, see Table I) is related to changes in the matrix composition and density included in the TRIDYN calculation. Effects of sputtering and oxide swelling are negligible (LD) or compensate each other (HD); thus, for each energy the position of the Ge peaks is independent of the fluences. The damage calculation [Fig. 1(b)] reveals that the near-surface displacement-per-atom (dpa) rate is always ≥ 1, i.e. each atom in the oxide matrix is displaced at least once on an average during implantation. About 70% of the implanted Ge is located within the region of strongly damaged oxide (defined by dpa > 0.3) between 6 and 16 nm depending on the energy. For samples of series A both the impurity and the damage profiles are far away from the Si substrate which avoids any influence of the Si/SiO_2 interface on the Ge redistribution and loss.

A. Ge loss during wet-chemical cleaning

As shown in Fig. 2(a), already a standard wet-chemical H_2O_2/H_2SO_4 cleaning treatment (CP1) after ion implantation reduces significantly the Ge content in SiO_2. The Ge loss increases with decreasing implantation energy, i.e. the loss increases as closer the implanted Ge is located to the surface. For a shallow Ge implant of 1.5 keV, 5×10^{15} cm^{-2} ($R_p = 4$ nm) almost all Ge gets lost after CP1-cleaning. A separation of the different steps involved in the cleaning sequence clearly reveals that the H_2O_2 component determines the Ge loss during cleaning [Fig. 2(b)]. An ultrasonic flushing in deionized water or in hydrocarbon solvents (like isopropyl-alcohol) solely have only a minor influence on the Ge loss. A cleaning treatment similar to CP3 but with boiling water (~ 100°C) in step 2 reproduces the result of CP2 which excludes a crucial influence of the cleaning temperature.

The significant Ge loss during H_2O_2/H_2SO_4 (CP1) cleaning can be explained as follows: During implantation nearly all Si and O atoms within a near-surface oxide region are displaced due to atomic collisions [Fig. 1(b)], which is associated with bond reconfigurations. The as-implanted Ge are bound preferably to oxygen atoms from the disturbed matrix or additional oxidizing species (O_2, OH etc.) penetrating into the damaged oxide after implantation. It has been shown by XPS studies that surfaces of Ge bulk material exposed to air oxidize to GeO_2 (oxidation state Ge^{4+})[27–29] whereas a mixture of different oxidation states (Ge^0, Ge^{2+}, Ge^{4+}) is observed for Ge implanted ($E > 100$ keV, $R_p > 70$ nm) thick SiO_2 films.[17,30,31] In our experiments, XPS of low-energy (1.5 keV) implanted samples (see Figs. 3 and 5) confirm GeO_2 (Ge^{4+}) as the dominant oxidation state of Ge. This is not surprising as the main part of the Ge is located in a very-near surface region ≤ 3 nm [cf. Fig. 1(a)]. Ge oxides or hydroxides differ with respect to their solubility in water: GeO or $Ge(OH)_2$ (Ge^{2+}) are more or less insoluble whereas GeO_2 (Ge^{4+}) has a high solubility.[32] H_2O_2 is a strong oxidizing reagent. In general, a cleaning procedure, which involves H_2O_2, transforms

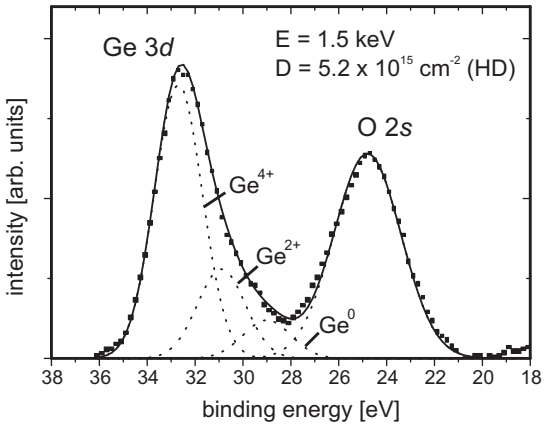


FIG. 3: XPS Ge $3d$ and O $2s$ data for the 1.5 keV, HD implant (as-implanted). The Ge $3d$ peak reveals a mixture of GeO_2 (Ge^{4+}), GeO (Ge^{2+}) and Ge (Ge^0) compounds (dotted) with binding energies of 32.7 eV, 30.9 eV and 29.0 eV, respectively which is about 0.9 eV per Ge-O bond (see Refs. 27,29,30). The O $2s$ peak centered at 24.8 eV corresponds mainly to oxygen from the SiO_2 network.

near-surface Ge, GeO, $Ge(OH)_2$ (Ge^0, Ge^{2+}) or similar components to GeO_2 (Ge^{4+}) and solute this oxide in H_2O (from $H_2O_2 \rightarrow H_2O + (1/2)\,O_2$) by forming H_2GeO_3.[32] It has been shown,[33] that the presence of oxygen is of vital importance for the dissolution of Ge in aqueous solutions. Although the oxidation state Ge^{4+} is already the major configuration after implantation and storage at humid air (Fig. 3), only minor Ge loss is obtained after flushing in cold or boiling H_2O contrary to a H_2O_2 treatment. This result indicates that the solution of GeO_2 embedded in the SiO_2 matrix (despite damaged) differs from those of natively oxidized Ge surfaces. It is obvious to assume that this difference is related to existing Ge-O-Si bonds which do not allow an efficient solution in pure water. Oxygen radicals from decomposing H_2O_2 provide a high amount of reactive oxygen to form H_2GeO_3. The process starts at the surface and proceeds into depth creating a porous structure due to the selective removal of solved Ge. A higher Ge content enables a better chemical attack, thus the Ge loss increases with implantation fluence [Fig. 2(a)].

B. Ge loss during annealing

During annealing a further Ge loss is obtained. As shown in Fig. 4 the Ge content decreases with annealing temperature, which indicates a thermally activated, i.e. reaction and/or diffusion controlled process of Ge loss. A higher percentage of Ge remains for a higher implantation depth. A fluence dependence becomes more significant the closer the Ge is located to the surface [Fig. 4(b)]. With a higher thermal budget the absolute Ge loss saturates at a level of about $4\times10^{15}\,cm^{-2}$ and $8\times10^{15}\,cm^{-2}$

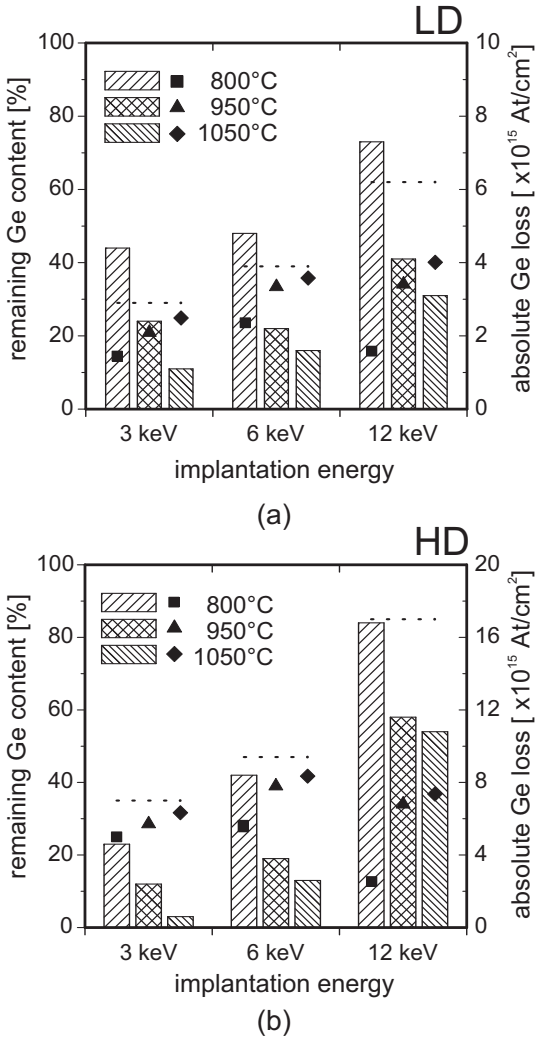


FIG. 4: Ge loss after RTA annealings in pure Ar for 30 s for LD (a) and HD (b) implants at energies between 3 and 12 keV (series A). The bar graphs belong to the left ordinate showing the remaining Ge content relative to the value after H_2O_2/H_2SO_4 cleaning. The corresponding absolute Ge loss and the total implanted fluence are indicated by symbols and a dotted line, respectively (right ordinate). The RBS measurements reveal minor differences between the implanted fluence and the initial parameters (see Tab. I).

for the LD and HD samples, respectively, if enough Ge is available. For the 1.5 keV, LD implant the residual Ge content decreases from 62% after cleaning to 40% of the initial amount already after annealing at 600°C for 10 min. As shown in Fig. 5 in this case only fully oxidized Ge (GeO_2, Ge^{4+}) and elemental Ge (Ge^0) remain after annealing. The Ge loss during annealing is attributed to intermediate Ge-O compounds with a mean binding energy of about 31.7 eV (cf. Ref. 27). This corresponds *e.g.* to a Ge^{3+} configuration, i.e. to Ge connected to three oxygen atoms with one dangling or Ge-Ge (Ge-Si) bond.

The Ge loss during annealing is supposed to be due

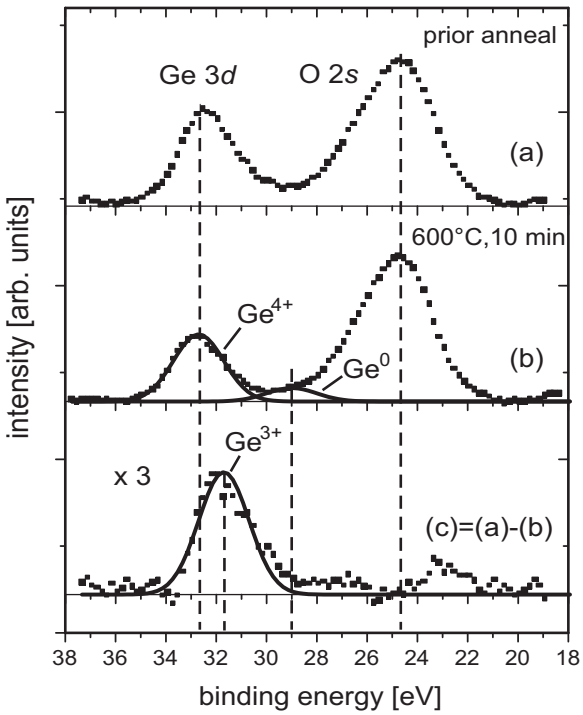


FIG. 5: XPS Ge $3d$ and O $2s$ data prior to (a) and after annealing at 600°C, 10 min (b) for 1.5 keV, LD implantation. The difference spectrum (c) of disappearing Ge during annealing is attributed to Ge^{3+} (31.7 eV).

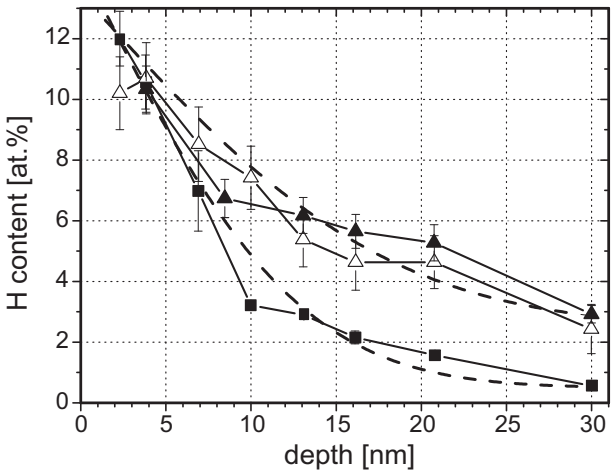


FIG. 6: Hydrogen depth profiles in SiO_2 obtained by NRA after ion implantation at 1.5 keV, LD (■) and 12 keV, HD (▲), the latter also after standard cleaning (△). Fitted profiles assuming a diffusionlike penetration [using the function $N(x)=N_0$ erfc $(x/2k)+c$ with the fitting parameter N_0, k, and c] are shown by dashed lines. A standard as-grown thermal oxide contains less than 0.5 at.% H (Ref. 20).

to the formation of volatile Ge compounds, i.e. GeH_4 or GeO. To form these compounds, excess hydrogen or oxygen atoms are required in the region of the implanted Ge. Two sources of excess oxygen and hydrogen can be defined. Firstly, ion implantation damages the oxide in a way that adsorbed water from humid air at the surface is able to penetrate the oxide by point-like H_2O or (after dissociation) by OH^- and H^+/H_3O^+ molecules.[20,34] The irradiation causes the formation of strained three-membered ring structures in the SiO_2 network, which are not stable for aqueous solutions.[35,36] The near-surface hydrogen (and oxygen) enrichment in the oxide after ion implantation is verified by NRA as shown in Fig. 6 for marginal implantation parameters. The hydrogen content decreases in depth in a diffusionlike manner without any visible accumulation in the region of the implanted Ge. The penetration depth (or the decay) is just correlated to the implantation energy, i.e., the depth of the modified oxide. The hydrogen profile is only weakly affected by the wet chemical cleaning treatment, thus the oxide is already conditioned after exposition to humid air subsequent to ion implantation. Secondly, the collision cascade and preferential sputtering during Ge implantation leads to local changes in the elemental oxide composition with respect to the SiO_2 stoichiometry. This process is only associated to oxygen related effects on the Ge loss and redistribution, whereas the penetration of additional hydrogen and oxygen (from humidity or as contaminants in the annealing ambient) into the oxide have to be considered to both, Ge oxide and hydride formations.

In the following exemplarily for the 12 keV Ge implants, where the highest remaining Ge contents are obtained in Fig. 4, the effects of excess oxygen and hydrogen on the loss and redistribution of Ge will be discussed in detail. The RBS data in Figs. 7(a) and 8(a) reveal that after annealing in pure Ar the Ge gets lost mainly from a region behind the profile maximum (HD) or rather homogeneously (LD) depending on the implantation fluence. The oxygen excess related to moisture is deduced from NRA data (Fig. 6) assuming a ratio H:O = 2:1. As calculated by TRIDYN, atomic collisions during ion implantation lead to an oxygen deficit close to the surface and an oxygen accumultation behind the implanted Ge profile [Fig. 7(b)]. Thus, the net oxygen excess can be calculated as presented in Figs. 7(b) and 8(b). The oxygen from moisture preferably saturates empty Si bonds and compensates the O deficit in the first 15 nm oxide depth for SiO_2 reconstruction during annealing. This process inhibits the formation of Ge oxides because $SiO_{2(s)}$ has a much higher heat of formation ($\Delta_f H^\circ$ = -910.7 kJ/mol) than $GeO_{2(s)}$ ($\Delta_f H^\circ$ = -580 kJ/mol) or $GeO_{(s)}$ ($\Delta_f H^\circ$,= -262 kJ/mol).[37] Only the net oxygen excess - obtained mainly behind the Ge profile in Fig. 7(b) - is supposed to react with the implanted Ge impurity atoms to form GeO during annealing. This GeO is mobile at elevated temperatures and escapes from the oxide surface toward the annealing ambient[27] (Ge loss) due to its high vapor pressure (about 1 mbar at 700 °C).[38–40] In a static balance of the calculated Ge content and the net oxygen excess the spatial

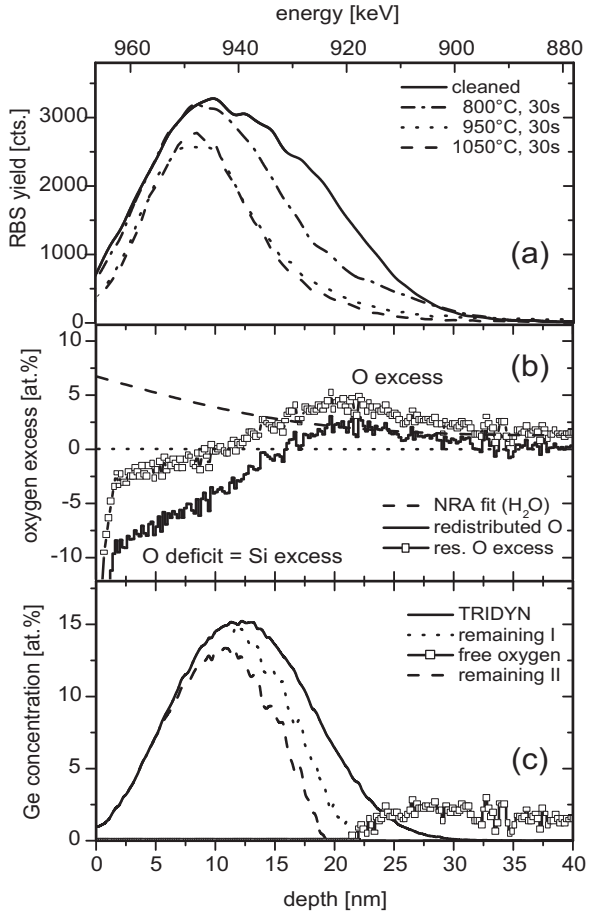


FIG. 7: Depth dependence of Ge loss during annealing for 12 keV, HD Ge implantation. (a) Ge profiles for different annealing temperatures as measured by RBS. (b) Total oxygen excess (squares) from a superposition of oxygen from H_2O indiffusion (dashed line) as obtained from NRA measurements (Fig. 6) with those - deficit or excess - generated during Ge implantation (straight line). (c) Profile changes (dotted line) due to a Ge loss by the formation of GeO with respect to the oxygen profile from (b) starting from the simulated implantation profile (straight line) [see Fig. 1(a)]. Remaining free oxygen (squares) according to the static approach causes further reduction of the Ge content during annealing (dashed line), which is considered to be more effective at the rear of the Ge implantation profile with a linearly decreasing impact toward the oxide surface.

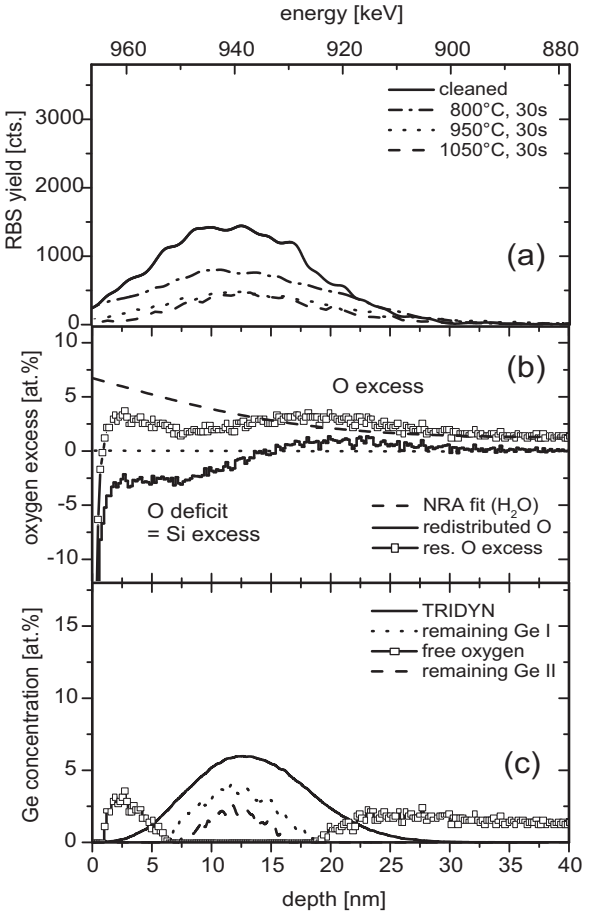


FIG. 8: Depth dependence of Ge loss during annealing for 12 keV, LD Ge implantation (notations as in Fig. 7). In (c) a homogeneous reaction is considered for simplicity, as "free oxygen" is available from both sides of the Ge profile.

Ge distribution changes as shown in Figs. 7(c) and 8(c) (denoted "remaining Ge I"). Such static approximations - both Ge and O are considered as locally fixed also during annealing - are likely in case of an oxygen deficient oxide as after implantation. Oxygen (and hydrogen) are presumably bound to Si and Ge forming ≡Si-OH[41] or ≡Ge-OH bonds (accordingly ≡Si-H and ≡Ge-H)[42–44] or being attached as H_2O.[45] However, some additional excess oxygen exist labelled as "free oxygen" in Figs. 7(c) and 8(c). This oxygen can be considered to be neither connected to Ge nor to Si in the SiO_2 network and is thus quite mobile during annealing. During diffusion toward the surface it reacts to remaining Ge or excess Si and reduces the Ge content further as indicated by "remaining Ge II" in Figs. 7(c) and 8(c). This estimation represents an upper limit of loss assuming the implanted Ge as the dominant sink for oxygen. For a lower Ge loss some oxygen might have left the oxide toward the ambient or is trapped at the Si bulk in the other diffusion direction. As a consequence, only the remaining Ge content is available for NC formation and determines the size and density of the corresponding NC's.

The model of GeO formation and emanation clearly reproduces the changes of the Ge profile shape after annealing as measured by RBS Figs. 7(a) and 8(a); Note, that the RBS depth profiles are superposed by the Si detector resolution (FWHM ≈ 15 keV) leading to a broadening of the Ge distribution. Furthermore, the calculated Ge losses are in reasonable agreement with the experimental values (LD/HD: calculated: 83%/33%, exp.: 69%/45%), which confirms the main assumptions of the model.

A similar calculation can be performed for a hydrogen related loss assuming the formation of volatile GeH_4 instead of GeO (see Fig. 9), but due to the Ge:H = 1:4

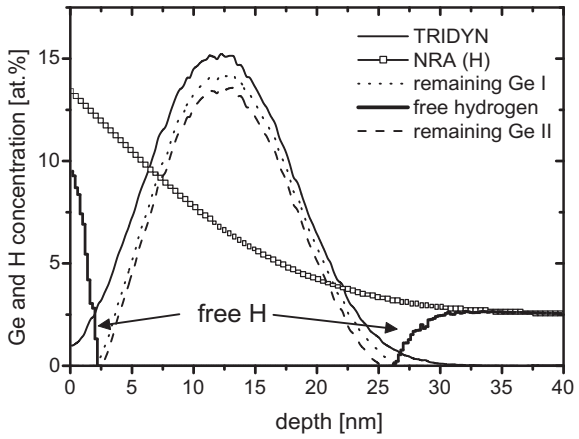


FIG. 9: Ge loss and redistribution due to GeH_4 formation simulated for the 12 keV, HD Ge implant. The initial hydrogen concentration (squares) is taken from NRA (Fig. 6). The simulation reveals negligible profile changes for both, the static and diffusion approximations. The initial Ge distribution is calculated by TRIDYN (straight line).

ratio the expected Ge loss is much lower ($\lesssim 20\,\%$) and does not reproduce the changed profile shape. In addition, from thermodynamics the formation of $GeO_{(g)}$ ($\Delta_f H^\circ$ = -46.2 kJ/mol) is favored compared to $GeH_{4(g)}$ ($\Delta_f H^\circ = +90.8$ kJ/mol)[37] during annealing if both reaction pathways are possible.

In summary the following reactions occur during annealing in pure Ar leading to the formation of volatile GeO.

For moisture components ($H_2O \longleftrightarrow H^+ + OH^-$):

$$2\,Ge + H_2O \longleftrightarrow \equiv Ge\text{-}H + \equiv Ge\text{-}OH \quad (2)$$

$$\longleftrightarrow Ge + GeO_{(g)}\uparrow + H_{2(g)}\uparrow \quad (3)$$

and for O excess caused by recoils:

$$Ge + (1/2)\ O_2 \longrightarrow GeO_{(g)}\uparrow\ . \quad (4)$$

The reactions stop if all excess O is consumed which is considered to be the reason for the saturating Ge loss for higher annealing temperatures [cf. Fig. 4(b)]. These considerations hold primarily for systems where the content of Ge in SiO_2 considerably exceeds the amount of reactive oxygen. Otherwise, as for 1.5 keV Ge implantation, the formation of GeO_2 is much more probable (cf. Figs. 3 and 5) which is completely miscible with SiO_2. In case Ge NC's are formed and just partially oxidized or passivated by a GeO_2 shell, a reduction might occur during annealing in oxygen deficient ambient by the formation of volatile GeO.[27,28,32]

$$Ge + 2\,H_2O \longrightarrow GeO_2 + 2\,H_{2(g)}\uparrow \quad (5)$$

$$Ge + GeO_2 \longrightarrow 2\,GeO_{(g)}\uparrow \quad (6)$$

As previously demonstrated in this paper, the Ge loss is mainly determined by the amount and distribution of

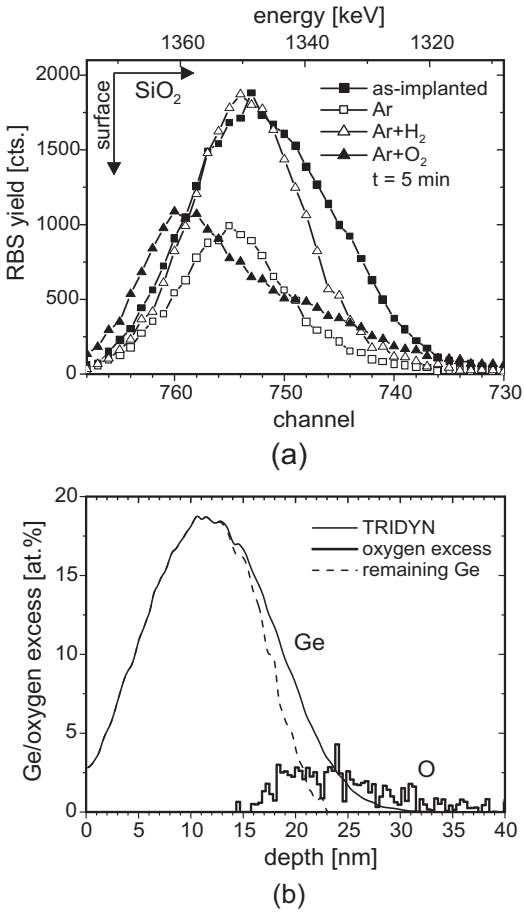


FIG. 10: (a) Ge distribution after annealing in Ar/H_2 or Ar/O_2 mixtures at 900°C for 5 min obtained by RBS. (b) Changes in the Ge profile taking only displaced oxygen during implantation into account. The data for the Ge content and O excess are obtained by TRIDYN calculations.

excess oxygen with respect to the position of the implanted Ge profile. Due to the strong influence of implantation and annealing parameters, an estimation of the Ge loss requires a modeling based on the most relevant processes with detailed knowledge of the experimental conditions. From the diffusion-like moisture distribution in SiO_2 as obtained by NRA a dominating Ge loss close to the SiO_2 surface would be expected. But in this region Ge is stabilized by an O-deficient oxide which consumes a significant part of the penetrating oxygen for the recovery of the SiO_2 network. The formation of small Ge precipitates or NC's in SiO_2 suppresses the Ge loss due to the self-limiting oxidation of small particles.[46] This might contribute to a smoother profile of the remaining Ge, but is not able to avoid the Ge loss in general.

C. Influence of annealing ambient and extended oxide damage

In the previous chapter due to annealing in ultra-pure Ar, we were capable to investigate solely the role of the "intrinsic source" (caused by the penetration of moisture after ion implantation) on the Ge loss and redistribution. Reactive species introduced by the annealing ambient had been excluded. In the second set of samples (series B, $d_{ox} \leq 100\,\text{nm}$) the annealing ambient has been enriched by a small amount of oxygen or hydrogen (see Tab. I) to stimulate the corresponding effects compared to annealing in ultra-pure Ar. The Ge implantation was performed at 12 keV, $1.8\times10^{16}\,\text{cm}^{-2}$ which is close to the 12 keV, HD implant of the preceding experiment (series A).

As shown in Fig. 10(a) annealing in pure Ar at 900°C for 5 min leads again to a considerable Ge loss (60%) with similar changes in the Ge profile shape as obtained before [cf. Fig. 7(a)]. Annealing in an oxygen containing ambient (Ar+5%O_2) causes a clear Ge redistribution toward the surface with a slightly lower total loss of about 40% of the initial Ge amount, whereas additional hydrogen (Ar+5%H_2) significantly reduces the loss to about 17%. In agreement to previous investigations[14–17] for annealing in oxygen containing atmosphere, GeO_2 has formed in a region close to the surface where the profiles of in-diffusing oxygen and out-diffusing Ge species (mainly GeO) overlap during annealing. An oxidation to GeO_2 fixes the volatile GeO within the oxide and reduces the total Ge loss.

$$2\,\text{GeO} + \text{O}_{2(g)} \longrightarrow 2\,\text{GeO}_2 \qquad (7)$$

In case of the formation of volatile GeH_4 in SiO_2 a much enhanced loss was expected during annealing in Ar+H_2, but contrariwise Ge seems to be immobilized in presence of hydrogen at least for 900°C annealing. About the reason for this behavior one can just speculate considering the present experimental data. With respect to moisture related loss [Eq. (2)], Ge-O compounds like ≡Ge-OH can be reduced by hydrogen to elemental Ge under emanation of H_2O.[47]

$$\equiv\text{Ge-OH} + (1/2)\,\text{H}_{2(g)} \longrightarrow \text{Ge} + \text{H}_2\text{O}_{(g)}\uparrow \qquad (8)$$

On the other hand the balance reaction in Eq. (3) might be weighted to the left side due to a significant partial pressure of H_2 in the oxide, which suppresses the formation of GeO by hindered release of gaseous H_2. In both cases the Ge loss due to the moisture related oxygen excess will be reduced. Assuming solely recoiled oxygen, the respective calculations illustrated in Fig. 10(b) validate the experimental results. The calculated Ge loss of 12% is very close to the experimental value of 17% also corresponding to profile changes. The recoiled excess oxygen oxidizes local Ge to GeO, which is apparently not affected by H_2 at 900°C. It seems to be plausible that a single weak Ge-OH bond (moisture) can be easier released by hydrogen than stronger Ge=O bonds (displaced oxygen).

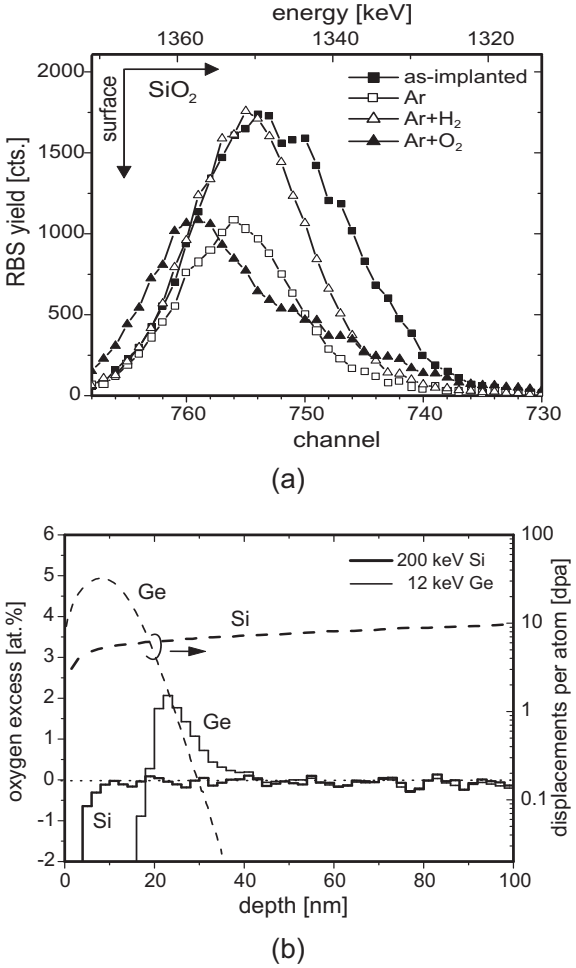


FIG. 11: (a) Ge distribution obtained by RBS for a consecutive 200 keV Si ($R_p = 280\,\text{nm}$) and 12 keV Ge implantation in 100 nm SiO_2 (series B) after annealing at 900°C for 5 min in different ambients. (b) TRIDYN simulation of the Si/Ge implantations according to stoichiometry changes between Si and O (oxygen excess). The dpa rate during implantation (dashed lines) is also shown and refers to the right ordinate.

In a different experiment a sequential 200 keV Si and 12 keV Ge implantation was carried out in 100 nm SiO_2 (cf. Tab. I) without braking the vacuum condition during implantation. As shown in Fig. 11(b) the number of dpa's exceeds about 5 across the whole oxide, whereas the content of implanted Si remains negligible (≤ 0.1 at.%). One could assume that a homogeneous irradiation of the entire oxide layer forces the penetration depth of moisture. But, as illustrated in Figs. 11(a) and 10(a), independent from the annealing ambient, almost the same Ge loss and redistribution is obtained after annealing in comparison to films without Si irradiation. The homogeneous oxide damage from the Si irradiation has apparently no impact on the total moisture content within the oxide. As shown in Fig. 11(b) the oxygen redistribution from

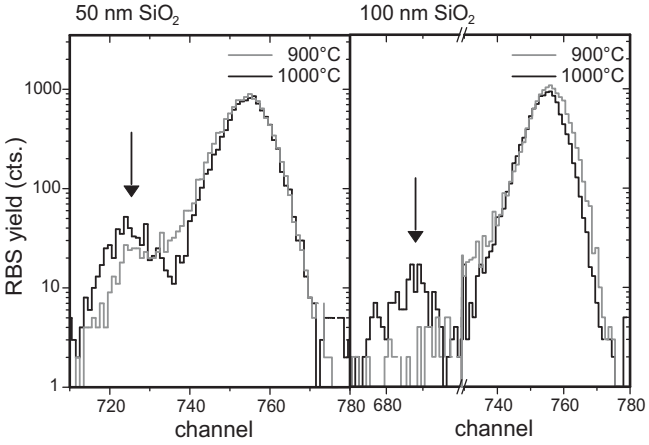


FIG. 12: Ge profiles from RBS after combined Si and Ge implantation in 50 nm (left) and 100 nm (right) SiO_2 films, annealed in pure Ar at 900°C and 1000°C for 5 min (series B). A distinct Ge amount is trapped at the Si/SiO_2 interface (marked by arrows). Nearly the same results were obtained for a single Ge implantation in 100 nm SiO_2 without Si irradiation.

atomic collisions during Si irradiation is negligible compared to the subsequent Ge implant. Thus, the penetration of moisture seems to be more related to the depth of sub-stoichiometric oxide as generated by Ge implantation, which reflects a higher amount of Si dangling bonds, than to the total number of dpa's [Fig. 11(b)]. Thus, the diffusion-like moisture profile in ion-irradiated SiO_2 might saturate even for a deeper oxide damage at a level similar to the hydrogen depth profile in Fig. 6 for 12 keV implantation.

IV. DIFFUSION OF Ge AND GeO IN SiO_2

A. Activation energy of diffusion

Besides mobilized Ge due to GeO formation there is no broadening of the remaining Ge profile as shown e.g. in Fig. 10(a) for annealing in Ar+H_2. This clearly indicates that for $T \leq 1000$°C elemental Ge has apparently a much lower mobility in SiO_2 than GeO. From our experiments a diffusion coefficient of $D \ll 10^{-16}\,cm^2/s$ at 900°C can be estimated. For substitutional Ge in amorphous silica glass, Minke and Jackson[48] determined the diffusivity to $D(900°C) = 2.6\times10^{-21}\,cm^2/s$ and $D(1000°C) = 2.2\times10^{-19}\,cm^2/s$ ($D_0 = 7250\,cm^2/s$; $E_A = 5.69$ eV) which enables a diffusion length of only a few nanometer for $T = 1000$°C. It is noteworthy that the activation energy for the self-diffusivity of Si in SiO_2 films is close to that value ($E_A = 5.34$ eV[49]) which indicates an unique diffusion mechanism probably slightly influenced by the different atomic radii (Si: 1.46 Å, Ge: 1.52 Å).

More detailed information concerning the activation energy for the diffusion of GeO can be derived from the Ge accumulation after annealing at the Si/SiO_2 interface as shown in Fig. 12. This accumulation is a common effect in Ge implanted SiO_2 films[13,15] caused by a condensation of Ge and O from diffusing GeO at the substrate surface according to Eq. (9).

$$Si + 2\,GeO \longrightarrow SiO_2 + 2\,Ge \qquad (9)$$

During annealing time t_a an areal density $m\,(T,\,t_a)$ of Ge atoms is trapped at the Si/SiO_2 interface, more precisely at the uppermost atomic layers of the Si substrate, in a distance Δx to the Ge profile. Accordingly, there the Ge concentration is initially $N_0 = 0$ with a constant gradient toward the Ge profile of $\Delta N(T) = N(T) - N_0$, i.e. no Ge is re-emitted from the Si substrate into the oxide. Assuming an uniform diffusion coefficient $D \neq D(x)$, a linearization of the Fick's first law yields

$$m(T,t) \;=\; D(T)\frac{\Delta N(T)}{\Delta x}\,t_a \;=\; \tilde{D}_0\,exp\left(-\frac{E_A}{kT}\right)\frac{t_a}{\Delta x}\,. \qquad (10)$$

The atomic concentration $N(T)$ of the diffusing Ge specie close to the Ge profile depends on the heat of formation for the corresponding chemical reaction. Thus, the total activation energy E_A includes both, the energy of formation and migration; $\tilde{D}_0$ is an effective prefactor of diffusion (unit: 1/cm s). From the RBS data in Fig. 12 in case of implantation in the 50 nm thick oxide $m(900°C) = 1.6\times10^{14}\,cm^{-2}$ and $m(1000°C) = 3.4\times10^{14}\,cm^{-2}$ can be easily deduced resulting in $E_A \approx 0.95$ eV. For 100 nm thick SiO_2 $m(900°C) \leq 3\times10^{13}\,cm^{-2}$ and $m(1000°C) = 1.0\times10^{14}\,cm^{-2}$ are obtained, but the first value indicates just an upper level as the amount of trapped Ge is below the detection limit. An respective activation energy of $E_A \geq 1.55$ eV indicates that the diffusivity of GeO is clearly influenced by the Si/SiO_2 interface whereas E_A increases with the distance of the Ge profile to the interface. A similar effect of the oxide thickness is reported for Si self-interstitial diffusion in SiO_2[50] and is explained by the emission of O vacancies (or SiO) from the interface (see also chapter IV.C).

B. Supposed mechanism of GeO diffusion in SiO_2

From our experiments GeO is identified as the mobile species in SiO_2 which explains both, the correlated Ge redistribution and loss. But the diffusion mechanism deserves closer attention, as the idea of a diffusing GeO molecule through the SiO_2 network is probably misleading. At elevated temperatures ($T \geq 900$°C), which are required for NC formation and oxide annealing, statistically breaking and re-forming of Si-O bonds occurs within the SiO_2 network including bond switching during relaxation. Thus, it is likely to assume that the GeO molecule is integrated into the covalent structure of SiO_2. In Fig. 13(a-c) a possible configuration for embedded GeO in the SiO_2 network is schematically shown neglecting

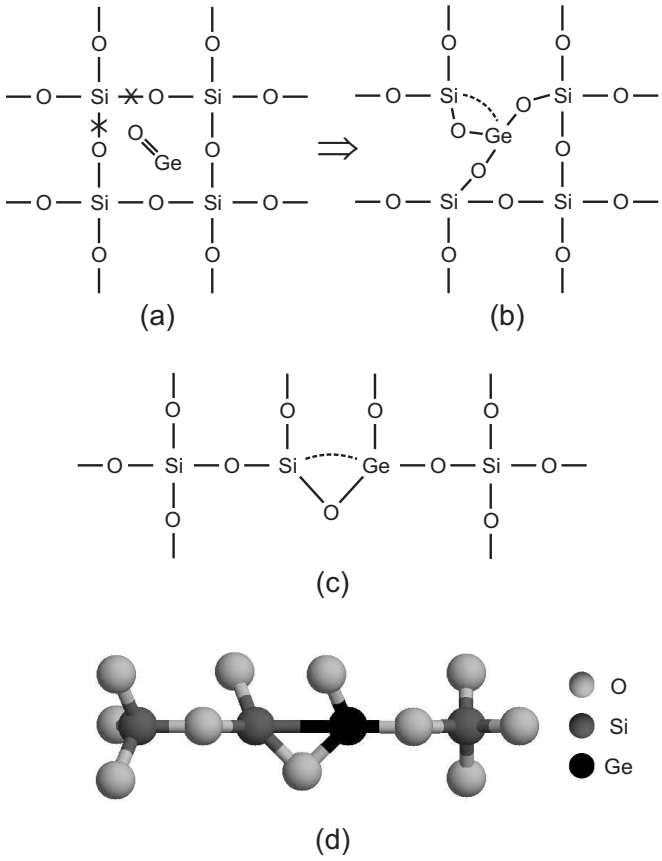


FIG. 13: Model for the introduction of a GeO molecule in the SiO_2 network. (a) Switching of two Si-O bonds (marked by crosses) leads to a reconfiguration as suggested in (b) by the formation of a bound Ge interstitial and an oxygen vacancy or to a probably more relaxed state as shown in (c). The latter configuration is similar to the triangular-oxygen-deficiency center in SiO_2 as proposed by Uchino *et al.*.[51] A 3d model of (c) is shown in (d) for instance with an interatomic distance of 1.6 Å and 2.38 Å for Si-O and Si-Ge, respectively,[52] and a Si-O-Si (Ge-O-Si) bond angle of about 144°.

the real tetragonal structure of the oxide. The switching of two Si-O bonds leads to a structure similar to a so-called Ge oxygen-deficient center (Ge ODC)[52] characterized by an oxygen vacancy (V_o) in combination with a substitutional Ge atom (S_{Ge}). Several possible models for an oxygen vacancy in SiO_2 are reported.[51,53,54] A configuration as in Fig. 13(c) with three oxygen bonds and one Ge-Si bond corresponds to a Ge^{3+} oxidation state as obtained in the XPS spectra in Fig. 5.

$$SiO_2 + GeO \longrightarrow S_{Ge} + V_o \tag{11}$$

Remember that with GeO also an extra O is introduced which migrates accompanied to the Ge ODC. But, along its way through the oxide, it is exchanged with oxygen from the relaxing SiO_2 network. If such a Ge ODC reaches the oxide surface, it emanates from the surface into the annealing ambient as a GeO molecule. In case O is present in the annealing ambient, the oxygen vacancy and thus the Ge ODC is annihilated forming "immobile" GeO_2 which is embedded in SiO_2. This state corresponds to the fixed Ge amount closer to the oxide surface as shown in Fig. 10(a).

In the temperature range up to 1000°C oxygen vacancies have a much higher mobility in SiO_2 than Si or Ge interstitials.[53,55] Previous experiments reveal that in Ge doped silica glass only Ge ODC's are observed or, in other words, the oxygen vacancies localize preferably near Ge atoms.[52,56] Si-Si related ODC's with neighboring Ge atoms are transformed in an exothermal reaction to Si-Ge related ones due the weaker Ge-O bond with an energy gain of $E_R \simeq 0.6\,\mathrm{eV}$.[52]

$$\begin{aligned} &\equiv\text{Si-Si}\equiv + \equiv\text{Si-O-Ge}\equiv \longrightarrow \\ &\equiv\text{Si-Ge}\equiv + \equiv\text{Si-O-Si}\equiv + \mathrm{E}_R \end{aligned} \tag{12}$$

The existence of such Ge related oxygen vacancy defects was confirmed at Ge implanted oxides by luminescence measurements.[57,58] The process of enhanced Ge diffusivity is similar to the well known transient enhanced diffusion of boron which is related to the diffusion of mobile Si self-interstitials in Si bulk material.[59] Here, the Ge impurity atom is connected to a highly mobile oxygen vacancy representing a diffusing Ge ODC complex. In that way the Ge atom gains a much higher diffusivity than a Ge interstitial alone. Recent investigations by Minke *et al.*[48] show that the activation energies for the diffusion of Ge and Si in SiO_2 are nearly equivalent which leads the authors to the suggestion that the diffusion mechanism is similar for both. Dangling bonds of the glassy matrix are supposed to be involved in the diffusion process instead of an Si or Ge interstitial motion. This clearly underlines the coherence of our model.

C. Role of Si/SiO_2 interface

The existence of a sub-stoichiometric SiO_x ($x < 2$) region close to the Si/SiO_2 interface is well-known and widely accepted in the microstructure of SiO_2 films on Si. This is equivalent to the presence of a high concentration of oxygen vacancies decaying with oxide depth.[60] The emission and diffusion of V_o is much more pronounced during annealing in an ambient with low or even negligible oxygen partial pressure.[61] As the O vacancies are essentially involved in Ge ODC's (shown before), the mobility of the Ge increases with the number of available oxygen vacancies. This explains the enhanced Ge mobility with decreasing distance of the Ge profile to the Si/SiO_2 interface as obtained from Fig. 12. Our calculated values for the activation energy of Ge migration of $E_A \approx 0.95\,\mathrm{eV}$ and $E_A \geq 1.55\,\mathrm{eV}$ approximate the reported value of oxygen vacancy migration of $E_A = 1.8\,\mathrm{eV}$[53] (from *ab initio* calculations according to an ideal oxide network) with increasing oxide thickness. Available oxygen vacancies support pathways for the Ge atoms diverging from the ideal model of oxygen vacancy migration. In the balance of

energies a contribution of formation ($E_A = 0.85\,\mathrm{eV}$ from *ab initio* calculations[62,63]) can be omitted as the detachment of Ge atoms from Ge precipitates in SiO_2 (which form already during Ge implantation) is mediated by an exothermal reaction similar to an oxidation to GeO.

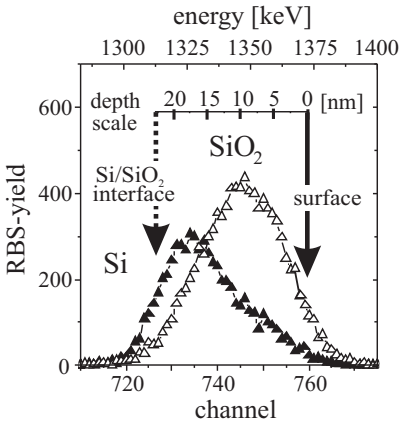
As a comparable effect, the self-diffusivity of Si in SiO_2 shows also a significant dependence on the oxide thickness.[50] The diffusivity increases with reduced oxide thickness, but this influence gets weaker if oxygen is introduced in the annealing ambient.[49,50] SiO molecules are discussed to be involved in the Si self-diffusion.[64–66] It was argued, that, especially during annealing at very low oxygen partial pressure, SiO molecules are emitted from the Si/SiO_2 interface into the oxide.[61] But, the explanation of the present results using GeO and SiO molecules instead of O vacancies leads to contradictions. The molecules would annihilate each other when they meet in the oxide region between the Ge profile and the Si/SiO_2 interface.

$$\mathrm{GeO} + \mathrm{SiO} \longrightarrow \mathrm{SiO_2} + \mathrm{Ge} \tag{13}$$

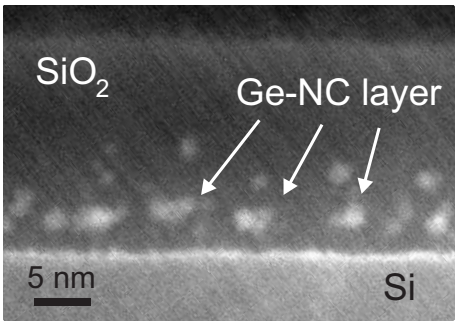
An unbound Ge interstitial would remain in SiO_2, which has a much lower diffusivity in SiO_2 than GeO as discussed before. The Ge diffusivity would tend to decrease with decreasing oxide thickness in contradiction to present results (Fig. 12). But, as mentioned by Stesmans *et al.*[54], the model of SiO in SiO_2 can conceivably be unravelled by the idea of a Si-Si oxygen vacancy in accordance to our structure hypothesis.[51]

$$\mathrm{SiO} \longrightarrow \mathrm{SiO_2} + \mathrm{V}_o \tag{14}$$

Migrating oxygen vacancies cause long-range distortions in the oxide network[52] leading actually to a Si self-diffusion in SiO_2. Penetrating oxygen in SiO_2 from the annealing ambient annihilates the oxygen vacancies and suppresses the Si self-diffusion. Thus, the Si self-diffusion in SiO_2 can be explained by a mechanism involving oxygen vacancies instead of SiO molecules or Si interstitials.



(a)



(b)

FIG. 14: Formation of a near-interface layer of Ge NC's in 20 nm SiO_2 after 5×10^{15} $^{74}Ge^{+}$-ions/cm^2 implantation at 12 keV and ion implantation (△) and annealing (▲). After annealing the major part of the Ge ($\sim 1.3\times10^{15}$ cm^{-2}) is located in vicinity to the Si/SiO_2 interface. A minor part is trapped at the Si substrate surface. (b) HAADF STEM image reveals separate Ge NC's of about 2 nm size, visible as bright spots, close to the Si/SiO_2 interface and some individual in the oxide bulk.

V. CONSEQUENCES OF THE Ge LOSS AND REDISTRIBUTION FOR A Ge NANOCRYSTAL MEMORY DEVICE

The significant mobility of Ge can be used for the formation of a self-organized Ge NC layer close to Si/SiO_2 interface which has been reported for Ge implanted gate oxides of 100 nm[10] or more device relevant of 20 nm thickness.[9,18] Such a near-interface NC layer is a desired configuration for Ge-nanocrystal-based memory devices.[3,4,9,11] The Ge redistribution due to volatile GeO or, in other terms, due to Ge ODC's during annealing in Ge implanted SiO_2 ($d_{ox} = 20$ nm) is illustrated in Fig. 14(a). The Ge loss, mainly occurring at the near-surface region, is about 30% of the implanted fluence after annealing at 950°C for 30 s.

Contrary to the Ge accumulation at the uppermost Si substrate shown in Fig. 12, here the Ge forms NC's within the oxide which is confirmed by TEM [Fig. 14(b)]. This process deserves a more detailed description. For IBS in thin gate oxides ($d_{ox} \leq 20$ nm), the implantation cascade usually meets the Si substrate resulting in a mixing of the Si/SiO_2 interface. During subsequent annealing (phase-)separation of Si and SiO_2 occurs associated with a complete interface reconstruction and a formation of tiny Si precipitates in the SiO_2 close to the Si/SiO_2 interface.[70] At these Si precipitates a significant amount of mobile Ge (from GeO) condenses [cf. Eq.(9)]. The high contrast of the bright spots in the TEM micrograph of Fig. 14 confirms that the NC's are composed mostly by Ge atoms, as such small Si NC's would be not resolvable by high-angle annual dark field (HAADF) scanning TEM. On the contrary to Ge interstitial diffusion, the migration of GeO-like complexes lead to an oxidation of the excess Si in SiO_2 confirming the formation of a nearly elementary pure Ge NC's layer.

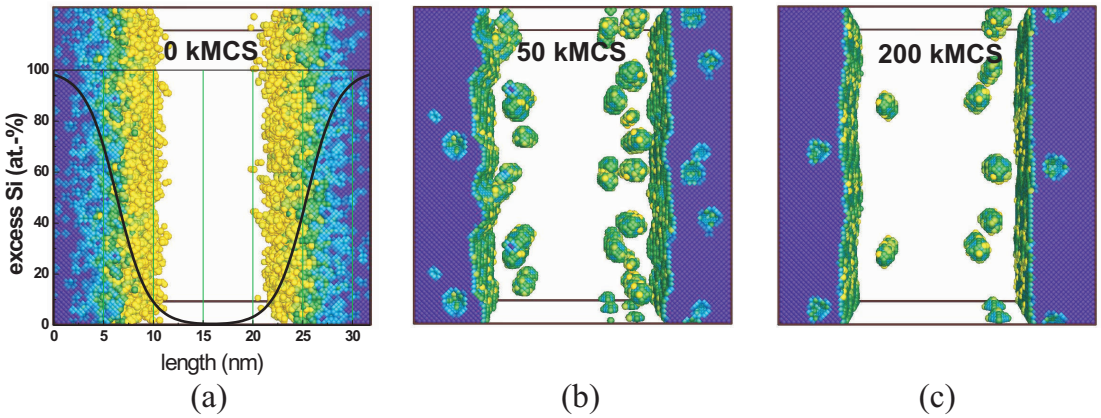


FIG. 15: Formation of a Si NC layer close to the Si/SiO_2 interface traced by 3D-KLMC simulation for a stack of 50 nm n^+-poly Si/15 nm SiO_2/(100)Si which is irradiated by 50 keV, 1×10^{16} Si^+-ions/cm^2. The gray scale/color reflects the number of diatomic Si-Si bonds. After 50000 MC steps Si NC's and SiO_2 clusters are formed in the SiO_2 and the Si bulk, respectively. Due to the higher mobility of O in Si than Si in SiO_2 the Si NC's are far more stable than the SiO_2 clusters in Si. With proceeding simulation/annealing time the Si/SiO_2 interface gets smoother and the NC's dissolve until a equilibrium of totally separated regions (SiO_2 and Si bulks) is reached. The KMC simulation was performed by K.-H. Heinig, Forschungszentrum Dresden-Rossendorf, and is presented with kind permission of the author and the publisher[3] (see also Refs. 67–69).

The process of interface reconstruction and formation of Si precipitates (or even NC's) in the oxide can be traced in a 3D-KLMC simulation as presented in Fig. 15.[3] As a model system, there a $Si/SiO_2/Si$ stack is treated by a Si irradiation. The Si excess in the oxide close to the Si/SiO_2 interfaces is achieved just by ion beam mixing, more or less independent on the kind of the implanted ions. During annealing the interfaces recover and a certain amount of mixed Si atoms remain within the SiO_2 forming precipitates which subsequently grow to Si NC's.

The influence of mobile Ge has to be carefully adjusted according to the right balance in processing between the presence of excess oxygen necessary for the Ge redistribution and the Ge loss, especially if a single NC layer is desired. Besides appropriate implantation conditions, special care has to be taken for the oxygen partial pressure in the annealing ambient which has to be quite low; otherwise GeO_2 formation in the gate oxide dominates. A small amount of hydrogen in the annealing ambient can be used to suppress the Ge loss. In addition subsequent thermal processes during device fabrication including hydrogen or oxygen containing species and/or post-IBS heat treatments may influence the NC's arrangement. The deposition of a capping layer like Si_3N_4 prior to implantation is not helpful because in this case oxygen from moisture is excluded which is needed for a considerable Ge redistribution.

VI. SUMMARY

A considerable Ge loss and redistribution is obtained during cleaning and annealing treatment of low-energy Ge implanted SiO_2 films, whereas the loss becomes more pronounced the closer the implanted profile is located to the oxide surface. A model for the diffusion of Ge in SiO_2 is given, which explains the high mobility of Ge in the oxide during annealing considering oxygen vacancies as the key diffusing elements. Ge loss and redistribution are strongly correlated to (i) a spatial modification of the oxide stoichiometry due to atomic relocations during ion implantation, and (ii) the penetration of additional oxygen and hydrogen species into the damaged oxide after implantation. Atomic collision during Ge implantation leads to a near surface oxygen deficit (i.e. Si enrichment) and an oxygen excess slightly behind the Ge implanted profile with respect to the initial SiO_2 stoichiometry. Additionally, moisture (H_2O vapor, H and OH) penetrates into the damaged oxide during storage at air, compensates a Si excess close to the oxide surface and enhances the oxygen excess in further depth. Thus, depending on the implantation parameters the overall oxygen (and hydrogen) excess in SiO_2 ("intrinsic source") is already conditioned prior to annealing. Apart from very shallow Ge profiles, where H_2O_2 containing cleaning chemicals cause a drastic reduction of the Ge content in the oxide by the formation of water soluble compounds (GeO_2, H_2GeO_3), the main Ge loss and redistribution occurs during subsequent annealing treatment. For neutral annealing ambients (e.g. Ar) the local ratio of Ge and excess oxygen within the oxide after ion implantation and cleaning determines, whether Ge is incorporated in the SiO_2 network as GeO_2, oxidizes to highly mobile GeO or remains as elemental Ge forming Ge NC's. A small amount of oxygen in the annealing ambient assists the formation of GeO and GeO_2, whereas an H_2/Ar annealing at 900°C significantly reduces the Ge loss probably due to a reduction of Ge oxides. During annealing the Ge loss is related to mobile GeO which diffuses toward the oxide surface and escapes there into the annealing ambient (or

the vacuum) due to its high vapor pressure. The diffusivity of GeO in SiO_2 ($D > 10^{-16}\,cm^2/s$ at 900°C) is orders of magnitude higher than of Ge interstitials. These considerations agree to the experimental result[15] that the Ge redistribution in SiO_2 is highly suppressed for samples protected by a diffusion barrier (e.g. Si_3N_4) prior to implantation avoiding a penetration of the damaged oxide by moisture or oxygen. GeO molecules in SiO_2 can be considered to be equivalent to Ge ODC's. Then, the diffusion mechanism is determined by the correlated Ge and oxygen vacancy movement through the oxide. As the Si/SiO_2 interface acts as an additional source of oxygen vacancies, the diffusivity of Ge is influenced by the oxide thickness, too.

Although a Ge loss is an undesired effect, with our findings and the diffusion model the high Ge mobility can advantageously be used to form a near-interface, δ-like Ge NC's layer in thin gate oxides for multidot memory devices. The diffusing Ge is trapped at Si nucleation centers close to the Si/SiO_2 interface which are formed as a result of interface mixing and phase separation during ion implantation and annealing, respectively.

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6 An electrical model of charging for nanocrystal containing gate oxides

A transient electrical model of charging for Ge nanocrystal containing gate oxides

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The write performance of a multidot-memory-like structure with respect to hole tunneling is investigated in MOS (metal-oxide-semiconductor) capacitors. The oxide of the MOS structure on p-type Si contains a layer of ion beam synthesized Ge nanocrystals (NC's) very close to the Si/SiO_2 interface. This structure is modeled in a floating-gate-like approach, where the NC's are considered as individual storage nodes and charged by direct tunneling of holes. Quantum confinement and Coulomb blockade effects of small Ge NC's (1 - 6 nm) are discussed and found to be negligible for the present structure. A close agreement between the calculated write characteristics and experimental data clearly confirms the validity of the model. From the simulation results it is predicted that a flatband voltage shift of about ΔV_{FB} = -1 V could be gathered with programming times $t_{prog} < 1\,\mu$s. The write parameters (pulse voltage and duration) for a given ΔV_{FB} value are mainly determined by the distance of the NC's to the substrate.

I. INTRODUCTION

Since the mid 90s the multidot memory has been of major interest in the research activities of emerging memory devices.[1,2] This memory concept is based on a layer of well separated Si or Ge nanocrystals (NC's) embedded in the transistor gate oxide substituting the floating gate of classical Flash-memory devices. Among various techniques for NC's fabrication[3] ion beam synthesis (IBS) has been established as a versatile method to produce a high density ($> 10^{12}$ cm^{-2}) of small (< 3 nm) Ge or Si NC's in thin gate oxides.[4,5] Multidot memories likewise promise short programming/write times ($t_{prog} < 1\,\mu$s), low operating voltages ($|V_{prog}| \ll 10$ V) as well as high endurance (10^9 cycles) with preferably long data retention.[2,6,7]

Previously, it was shown that in thin SiO_2 films IBS enables the formation of a self-organized, δ-like layer of Ge NC's close to the Si/SiO_2 interface.[4,8,9] In this paper, the write performance of such Ge NC's containing gate oxides is investigated by means of MOS (metal-oxide-semiconductor) capacitors. As the charge transfer occurs in the direct tunneling (DT) regime, charging by holes (instead of electrons) offers the advantage of an enhanced data retention due to the higher tunneling barrier ϕ_b.[10] We studied the time dependence of hole charging under substrate accumulation conditions. The evaluation is based on capacitance-voltage (C-V) measurements of MOS capacitors which restrict the programming time to $t_{prog} \gtrsim 3$ ms. To predict the performance for shorter programming times ($t_{prog} <$ ms), the experimental study is accompanied by simulations using a physical / electrical model of the device structure.

II. EXPERIMENTAL DETAILS

The MOS capacitors with a Ge NC containing gate oxide were prepared as follows: $^{74}Ge^+$-ions (12 keV, 5×10^{15} cm^{-2}) were implanted at room temperature in 20 nm thick oxide thermally grown on <100> p-type Si with a resistivity of $\rho = 10\,\Omega$ cm. After a standard cleaning step in H_2O_2/H_2SO_4 rapid thermal annealing (RTA) was carried out at 950°C for 30 s in Ar to recover the damaged oxide and to form the NC's. Afterwards, metal dots (A = 0.1 mm^2) were fabricated by Al-sputtering, photolithographic patterning and a 400°C, 15 min furnace anneal in N_2.

The Ge profile and the corresponding NC distribution in the gate oxide were characterized by Rutherford backscattering spectrometry (RBS) and scanning transmission electron microscopy (STEM), respectively. The RBS spectra were obtained by 1.7 MeV He^+-ions at a scattering angle of 170° and an incident angle of 70° to improve the depth resolution. The STEM analysis was carried out using a high-angle annular dark-field (HAADF) detector (acceptance angle about 2.8°) in a FEI Tecnai 20 FEG microscope operating at 200 kV. The C-V characteristics of the MOS capacitors were measured by a Keithley 590 CV analyzer at 100 kHz using a Keithley 237 voltage source as an external programming square-pulse generator. The measurement sequence

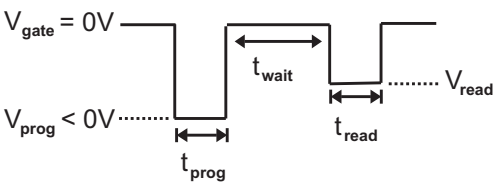

FIG. 1: Sequence of applied voltage pulses to investigate the write and retention characteristics of MOS capacitors.

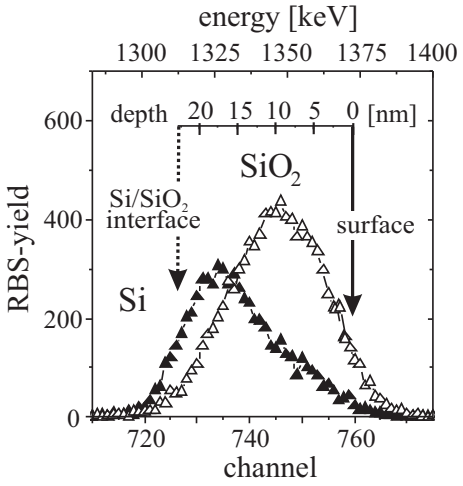

FIG. 2: Ge profiles after ion-implantation (△) and annealing (▲) as measured by RBS. After annealing the major part of the Ge ($\sim 1.3\times10^{15}\,\mathrm{cm}^{-2}$) is located in vicinity to the Si/SiO_2 interface. During annealing ∼30% of the implanted Ge amount gets lost by the formation of volatile species (mainly GeO).

is shown in Fig. 1. The MOS devices were charged by negative gate voltage pulses (-3 V ≥ V_{prog} ≥ -8 V) with durations of 3 ms ≤ t_{prog} ≤ 30 s. After t_{wait} = 1 ms at the reference potential of 0 V, a read pulse was applied with $|V_{read}|<|V_{prog}|$ for $t_{read} = t_{prog}$ while the C-V data $C(V_{read})$ are recorded. V_{read} is adjusted in such a way that at the beginning of the read-cycle $C(V_{read})$ is about $C_{FB}(V_{FB,0})$ which avoids an influence of the reading process on the charge state of the NC's after programming. C_{FB} denotes the flatband capacitance and $V_{FB,0}$ the flatband voltage of the initial (uncharged) MOS capacitor. Thus, the flatband voltage shift - as a measure of the stored charge - is easily obtained as $\Delta V_{FB} = V_{read} - V_{FB,0}$. Profiting from a short data retention (∼s) and a high endurance this procedure was repeated for each data point (V_{prog}, t_{prog}). The retention data are obtained for a single programming pulse with t_{prog} = 100 ms and a series of adapted V_{read} pulses with prolonged t_{wait} in between.

III. RESULTS AND DISCUSSION

A. Structural characteristics of the Ge NC layer

To enable a calculation of the charging characteristics $\Delta V_{FB} = f(V_{prog}, t_{prog})$, the size, density, and position of the NC's had to be specified as input parameters for the transient model. The initial (as-implanted) Gaussian-shaped Ge profile is centered in the oxide with a peak concentration of about 7 at.%. As obtained from RBS in Fig. 2 during annealing a significant Ge redistribution takes place towards the Si/SiO_2 interface. A layer of separated Ge NC's forms in the oxide close to the interface as confirmed by STEM imaging (see Fig. 3). This effect is a characteristic feature for Ge NC formation by IBS in thin SiO_2 films; its physical origin has been described elsewhere.[8,9] For the near-interface NC's a mean size of $d_{nc} \approx 2$ nm and a density of $N_{nc} \approx 1\times10^{12}\,\mathrm{cm}^{-2}$ as a lower limit can be deduced from STEM. For a total oxide thickness of 23 nm the tunneling oxide thickness d_{tox} varies between about 1 and 2.5 nm. An upper limit of the NC density of $N_{nc} \approx 7\times10^{12}\,\mathrm{cm}^{-2}$ can be estimated from RBS if the amount of near-interface Ge ($1.3\times10^{15}\,\mathrm{cm}^{-2}$) contributes to equal sized NC's of 2 nm. Assuming $N_{nc} \approx 3\times10^{12}\,\mathrm{cm}^{-2}$ and d_{tox} = 2 nm the mean distance between adjacent NC's is 3.8 nm. This is about twice the distance to the substrate which clearly favors the charge exchange with the substrate and prevents charge dispersion between NC's. The subsequent 400 °C anneal is negligible concerning NC size and distribution.

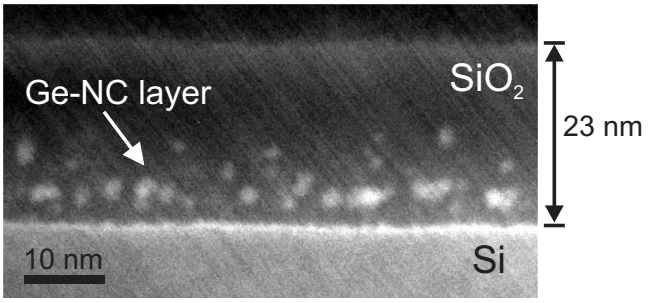

FIG. 3: Cross-sectional HAADF STEM micrograph after Ge implantation and annealing. A layer of separate Ge NC's formed close to the Si/SiO_2 interface with individual distance to the Si substrate. Some NC's are located in the oxide bulk. The bright spots confirm that the NC's consist mainly of Ge since Si NC's in SiO_2 would have a much weaker contrast. A proof of crystallinity succeeded for a similar sample with a higher Ge content using the same annealing conditions (950 °C, 30 s).[9]

B. Modeling of the transient programming characteristic

For Si implanted gate oxides Kalnitsky *et al.*[11] supposed that the charging is attributed to traps or defect centers whereas their distribution follows the implantation profile. This approach neither consider the formation of NC's in the oxide nor the elemental redistribution during annealing which is characteristic for Ge implanted oxides.[9,12] Here, the MOS structure is electrically modelled in a floating-gate-like approach[13,14] with a narrow distribution of equal-sized Ge NC's in the gate oxide. The NC's are considered as storage nodes (Fig. 4) subsumed in a layer with capacitances towards the substrate and gate electrode C_{tox} and C_{cox} representing the tunnel- and the control-oxide, respectively. For negative

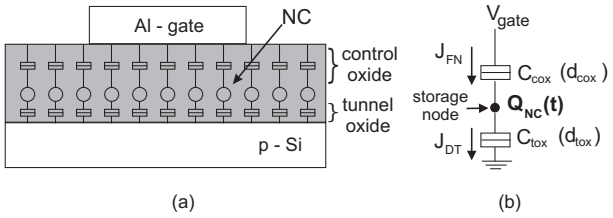

FIG. 4: (a) Structure model of a NC containing MOS diode. (b) Equivalent circuit for one NC as a floating storage node (schematics derived after Ref. 18).

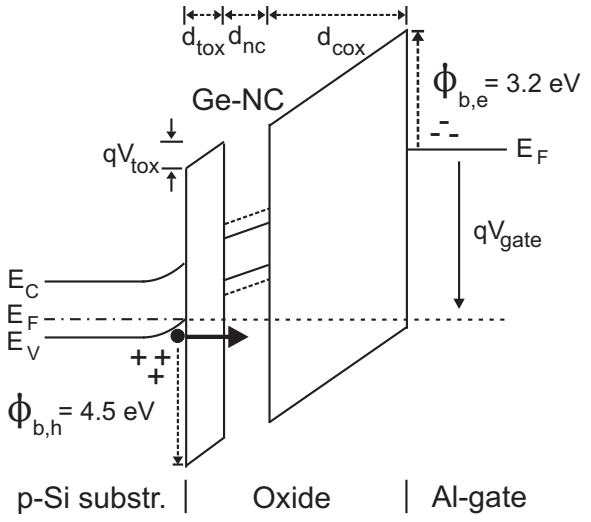

FIG. 5: Band diagram of a MOS structure with a Al-gate and a Ge NC's containing gate oxide for a negative gate voltage. Hole-DT from an accumulated p-Si substrate towards the NC's is shown. Dotted lines adumbrate a larger bandgap due to quantum confinement of the Ge NC's.

programming voltages (V_{prog}) holes are transferred by direct tunneling (DT) from the accumulated p-Si substrate towards the Ge NC's. V_{prog} is limited to low fields ($E_{ox} < 7\,\mathrm{MV/cm}$) to avoid Fowler-Nordheim (FN) injection of electrons or holes. Thus, the total current density simplifies to DT of holes J_{DT}[15,16]

$$J_{DT} = \frac{q^3 (m_{si,h}/m_{ox,h})}{8\pi h \phi_{b,h}} E_{tox}^2 \Theta_{tox} \qquad (1)$$

whereas the transmission probability Θ_{tox} for holes through the tunneling oxide for a parabolic dispersion relation in the Wentzel-Kramers-Brillouin (WKB) approximation is given by[15,17]

$$\Theta_{tox} = exp\left(-\frac{8\pi\sqrt{2m_{ox,h}}\left[\phi_{b,h}^{3/2} - (\phi_{b,h} - |qV_{tox}|)^{3/2}\right]}{3hq|E_{tox}|} \right) . \qquad (2)$$

Here, h denotes Planck's constant, q the elementary charge, m_0 the free electron mass, V_{tox} and $E_{tox} = V_{tox}/d_{tox}$ are the voltage drop and the electric field across the tunneling oxide, respectively. A schematic band diagram is shown in Fig. 5. In Eq. (1) the hole effective mass in the Si substrate $m_{si,h}$ is set to $\sim m_0$ taking into account heavy holes ($m_{hh} = 0.49 m_0$) as well as light holes ($m_{lh} = 0.16 m_0$) and split-off holes[19] ($m_{sh} \approx m_{lh}$). This is equivalent to a free Fermi gas of holes in the emitting electrode which is a reasonable approximation for accumulation conditions. Suitable values for the tunneling barrier of holes $\phi_{b,h}$ and the effective mass of holes in the oxide $m_{ox,h}$ in Eqs. (1) and (2) were extracted from current-voltage characteristics given in Refs. 19–21 (see Fig. 6). Relevant data for valence band hole tunneling can only be achieved from inverted p-MOS devices at gate voltage magnitudes less than 2V.[17,22,23] The best fit for the low bias range is achieved for $\phi_{b,h} = 4.5\,\mathrm{eV}$ and for $m_{ox,h} = 0.32\, m_0$ in agreement with a semi-empirical approach by Lee and Hu[17] for hole valence band tunneling. The small mismatch in Fig. 6 is attributed to a slightly differing V_{gate}-V_{ox} relation due to the depletion effect in the p^+-poly gate in p-MOS devices (we use an Al gate) and/or to the different hole emission from an inverted n-type substrate instead from a p-Si substrate in accumulation.[17] The lower barrier height in comparison to the widely used value of 4.8 eV (e.g. Ref. 24) is attributed to confined energy levels of holes at the Si/SiO_2 interface due to a narrow potential well (carrier confinement) for charge carrier accumulation within the Si substrate.[16,25–27]

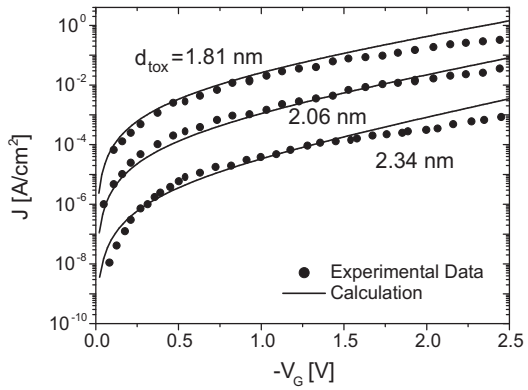

FIG. 6: Calculated DT hole currents according to Eqs. (1) and (2) for three different oxide thicknesses in comparison to experimental data from Refs. 19–21.

As the effective NC charge density Q_{nc} according to the whole capacitor surface is implicitly given by the integral over J_{DT}[14] (which is itself a function of Q_{nc}), the time-dependent (transient) charging process of the NC's is calculated iteratively as

$$Q_{nc}(t_{i+1}) = Q_{nc}(t_i) + R_{nc} J_{DT}(V_{tox}, Q_{nc}(t_i)) \Delta t \quad . \qquad (3)$$

$R_{nc} = (\pi/4)\, d_{nc}^2 N_{nc}$ represents the relative part of the capacitor area covered by Ge NC's. Equation (3) holds for small time increments Δt if the potentials within the gate oxide do not change significantly between the time steps

t_i and t_{i+1}. The voltage drop across the tunneling oxide V_{tox} depends on the coupling factor k, the NC charge Q_{nc} and the reduced applied gate voltage V'_{gate} (neglecting the Si surface potential and the work function difference between Al-gate and p-Si substrate as constant factors in the simulation) according to[13,14]

$$V_{tox}(t_i) = k\left(V'_{gate}(t_i) + \frac{Q_{nc}(t_i)}{\varepsilon_{ox}/d_{cox}}\right) \quad (4)$$

$$\text{with} \quad k = \frac{d_{tox}}{d_{tox} + (\varepsilon_{ox}/\varepsilon_{nc})\, d_{nc} + d_{cox}}\,. \quad (5)$$

To the benefit of simplified equations the charge is centered at the interface between the NC's and the control-oxide. Correspondingly ΔV_{FB}(t) can be calculated with Q_{nc}(t) from Eq. (3) by

$$\Delta V_{FB}(t_i) = -Q_{nc}(t_i)\, d_{cox}/\varepsilon_{ox}\,. \quad (6)$$

From the physical point of view, the NC's are characterized by their size d_{nc}, their dielectric constant $\varepsilon_{nc} \simeq \varepsilon_{Ge}$, their density N_{nc} and their position with respect to the Si/SiO_2 interface, i.e. d_{tox}. The latter one has the strongest influence on the charging behavior. Ion beam mixing at the Si/SiO_2 interface during implantation, phase separation, and Ge redistribution are statistical processes leading to a spatial distribution of NC's characterized by a variable distance of the NC's to the Si substrate, i.e. each d_{tox} corresponds to a number of NC's with different values of $Q_{nc}(t)$ and J_{DT}. In the calculations this spatial variation has been considered by a normalized Gaussian distribution of d_{tox} with a standard deviation of σ.

In the preceding considerations quantum confinement and Coulomb blockade effects of the small Ge NC's are hitherto disregarded which requires a more detailed comment. It is well known that quantum confinement leads to quantization of the energy levels and to an increase of the bandgap with decreasing NC size,[28] e.g. 3.5 eV exciton energy for Ge NC's of 2 nm size assuming a simple infinite potential well.[29] However, is has been shown that the effective bandgap strongly depends on the kind of surface passivation,[30–32] especially for very small NC's. This is not surprising as a NC of 2 nm size contains only 185 atoms and about 60% of them are surface atoms with at least one bond towards oxide matrix atoms. In general, surface passivation with hydrogen or oxygen lowers considerably the bandgap value. From theoretical considerations using the tight-binding approximation, Ge NC's of 2 nm size with H-terminated surface atoms exhibit a bandgap of 2.35 eV.[30] The ground state levels of valence and conduction band side shift almost symmetrically by $\sim$0.85 eV with respect to the bulk levels. A recent study shows that the bandgap of 2 nm NC's embedded in SiO_2 quenches to just about 1.1 eV.[33] In the present device the bandgaps of bulk Si and Ge NC's are aligned to each other according to their electron affinity, which differs for bulk values just slightly (4.05 eV and 4.0 eV related to the vacuum level, respectively). In this case the valence band edges of the Si and the Ge NC side differ by

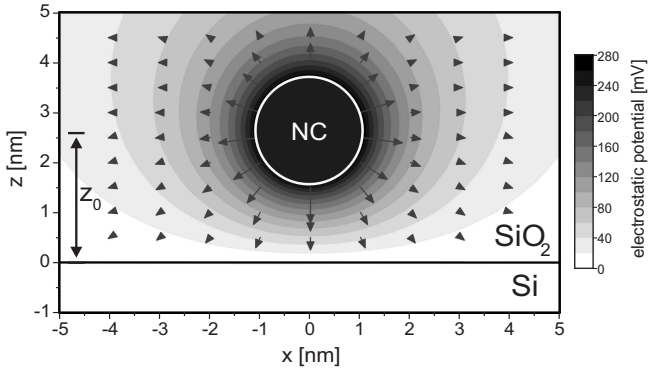

FIG. 7: Potential distribution for a positively charged (one hole) NC embedded in SiO_2 in a distance between NC center and conducting plane of z_0 with $\varepsilon_{nc} \gg \varepsilon_{ox}$ ($d_{nc} = 2$ nm and $d_{tox} = 1.6$ nm). The respective electrical fields are indicated by arrows.

0.5 eV without a barrier for hole tunneling towards the NC's (cf. Fig. 5). Taking quantum confinement of small oxygen passivated Ge NC's into account, the difference on the valence band side lowers to about 0.25 eV, but is still existing. Thus, for hole charging enough chargeable states in the NC's valence band are available despite the increase of the Ge NC's bandgap due to quantum confinement.

With respect to the Coulomb blockade effect the electrostatic charging energy of a single NC is given by $E = q^2/2C_\Sigma$. A threshold voltage of $\Delta V = q/C_\Sigma$ is needed to populate the island stepwise by one additional charge. C_Σ includes the parasitic capacitances to the Si substrate, to adjacent NC's in plane and to the gate. With respect to a single spherical charged NC above a conducting plane one gets

$$C_\Sigma \approx 4\pi\varepsilon_{ox} r_0 \frac{(2z_0 - r_0)}{2(z_0 - r_0)} = 4\pi\varepsilon_{ox} r_0 \left(1 + \frac{r_0}{2d_{tox}}\right) \quad (7)$$

with $z_0 = d_{tox} + r_0$ and the radius r_0 of the NC (see Fig. 7). The total capacitance of two conductive spheres of equal size can be obtained by the image charge method with one grounded sphere and one taking a point charge q [see Fig. 8(a)].[34] After full charge compensation the total charge q_Σ on the NC of interest is

$$q_\Sigma = q\left[1 + \frac{r_0^2}{(a^2 - r_0^2)} + \frac{r_0^4}{a^2(a^2 - 2r_0^2) - r_0^2(a^2 - r_0^2)} + ...\right]$$
$$\approx q\sum_{n=0}^{\infty}\left(\frac{r_0}{a}\right)^{2n} = q\left[1 + \frac{r_0^2}{(a^2 - r_0^2)}\right] \quad \text{for } a^2 \gg r_0^2$$

possessing the potential of $\varphi_0 = q/(4\pi\varepsilon_{ox} r_0)$ with $C_\Sigma = q_\Sigma/\varphi_0$. The approximation $a^2 \gg r_0^2$ locates the image charges at the NC's center neglecting small higher order terms.

The ensemble of two spheres can be expanded to a line and later on to an array of spheres as shown in Tab. I. The charge q in the central sphere has to be mirrored at

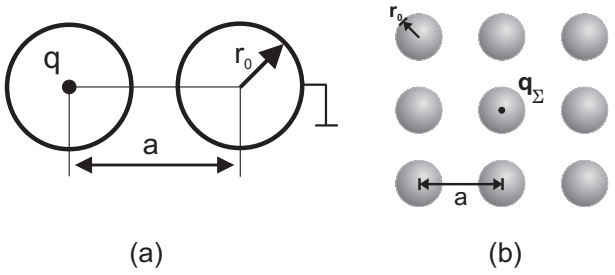

FIG. 8: (a) Two NC's symbolized by conducting spheres in distance a, whereas one posses the charge q and the other is grounded. (b) Array of NC's with their image charges in plan view.

TABLE I: Total capacitance C_Σ in aF of the charged sphere of interest (•) for an ensemble of spheres with $r_0 = 1$ nm and $a = 5$ nm ($N_{nc} = 4\times10^{12}$ cm^{-2}) comparing the exact calculation with approximations.

ensemble of spheres	•	•○	○•○	○○•○○	○ • ○	○ ○ ○ • ○	○ ○ ○ ○ • ○ ○ ○ ○
exact	0.434	0.453	0.470	0.473	0.494	0.500
$a^2 \gg r_0^2$	0.434	0.452	0.468	0.471	0.491	0.498
Eq. (8)	-	-	-	-	-	0.506

each island, but image charges there have also to be compensated with respect to the others to keep zero potential surface there introducing again image charges *etc.* The transition from a string of three spheres to five shows a negligible capacitance contribution of more distant ones. This leads to a nearest neighbor approximation with an array of NC's as shown in Fig. 8(b). For the same reason this ensemble can be reduced to a cross-like arrangement of five spheres. Thus, the total capacitance related to the central one for the full array results in

$$q_\Sigma \approx q\left[1+\frac{4\,r_0^2}{(a^2-r_0^2)}\right] = C_\Sigma\,\varphi_0 \quad . \tag{8}$$

But these charges have also to be mirrored at the conducting plane in parallel to the array of spheres. Equation (7) was deduced just for a single sphere possessing one charge. The sphere of interest within the NC array is now enriched with image charges by a factor of q_Σ/q. This yields

$$C_\Sigma \approx 4\pi\varepsilon_{ox} r_0\left(1+\frac{r_0}{2d_{tox}}\right)\left[1+\frac{4\,r_0^2}{(a^2-r_0^2)}\right] \tag{9}$$

neglecting the far distant gate electrode ($d_{cox} \gg d_{tox}$). These simple equations are no more valid for much larger, closely packed NC's ($d_{nc} > 10$ nm).[35] In the floating gate approach one charge per cm^2 shifts the potential of the NC layer like a Coulomb blockade of $V_{fg} \approx Q_{nc}/(\varepsilon_{ox}/d_{tox})$ for $k \approx d_{tox}/d_{cox}$ [cf. Eq. (4)].

TABLE II: Key parameters for the Coulomb blockade effect of equally sized Ge NC's ($d_{nc} = 2$ nm) embedded in SiO_2 with respect to one. C_Σ/C_{fg} is calculated for $N_{nc} = 3\times10^{12}$ cm^{-2} after Eq. (10).

d_{tox} [nm]	C_Σ [aF]	$E = e^2/2C_\Sigma$ [eV]	C_Σ/C_{fg}
1.0	0.73	0.110	0.64
1.5	0.65	0.124	0.85
2.0	0.61	0.132	1.06
2.5	0.59	0.137	1.27
3.0	0.57	0.141	1.48
3.5	0.56	0.144	1.70
4.0	0.55	0.147	1.91
∞	0.49	0.164	0.75[a]

[a]Related to the self-capacitance $C_\Sigma = 4\pi\varepsilon_{ox} r_0$ ($d_{tox} = 2$ nm).

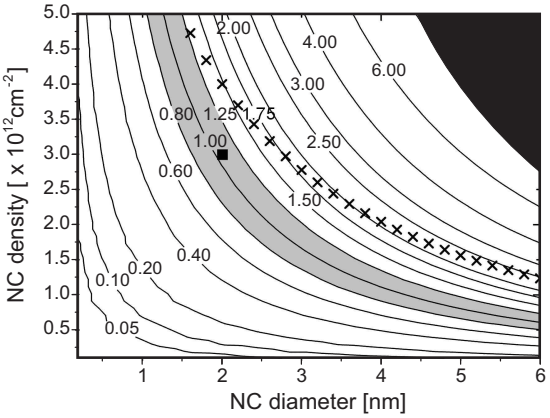

FIG. 9: C_Σ/C_{fg} ratio as a function of NC size and density for $d_{tox} = 2$ nm after Eq. (10). The floating gate approach is mainly valid for NC densities and sizes as marked by the gray area which is also the case for the present structure [$d_{nc} = 2$ nm and $N_{nc} = 3\times10^{12}$ cm^{-2}(■)]. Assumedly above $N_{nc} = 1/(3\,\text{nm} + d_{nc})$, i.e. for an inter-NC distance smaller than 3 nm, charge dispersion between the NC's has to be taken into account (×). The consideration of overlapping NC's is not appropriate (black area).

Thus, the relative capacitance per NC as shown in Fig. 4(a) is $C_{fg} \approx (\varepsilon_{ox}/d_{tox})\,(1/N_{nc})$. The floating gate approach can be used to describe the charging processes in NC based memory devices if C_Σ is close to C_{fg} which is valid for the present structure (cf. Fig. 9 and Tab. II).

$$\frac{C_\Sigma}{C_{fg}} = 2\pi\,r_0\,(2d_{tox}+r_0)\,N_{nc}\left[1+\frac{4\,r_0^2}{(1/N_{nc})-r_0^2}\right] \tag{10}$$

As a conclusion, quantum confinement and Coulomb blockade related effects are of minor influence for the writing characteristics of the system considered here and have not been included in the model as also argued by de Salvo *et al.*[13]

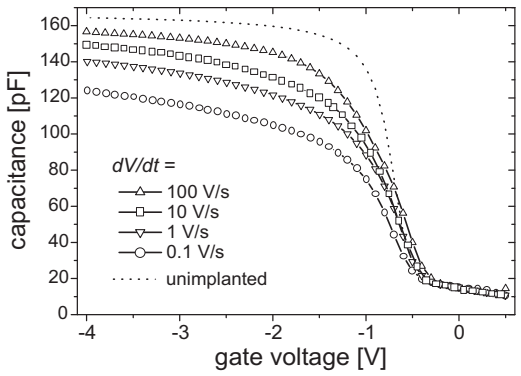

FIG. 10: C-V characteristics of the MOS structure with Ge NC's for different sweep rates dV/dt in comparison to the unimplanted reference (sweep direction: 0.5 V → -4.0 V).

C. Simulation Results versus Experimental Data

The measured C-V characteristics of the MOS capacitor containing Ge NC's strongly depends on the sweep rate which is not obtained for the unimplanted MOS reference (see Fig. 10). The capacitance increases just slowly for a conventional sweep rate of 0.1 V/s and does not achieve the maximum value $C_{ox} \sim 1/\, d_{ox}$ even at $V_{gate} = $-4 V. With increasing sweep rate the measured characteristic approaches the one of the unimplanted reference. This behavior becomes plausible, if one assumes a simultaneous charging during measurement: During the sweep the Ge NC's are successively charged by holes in accumulation conditions ($V_{gate} \lesssim$-1 V) leading to a shift of the real C-V characteristic which follows the applied gate voltage during measurement. With increasing sweep rate the amount of charge decreases resulting in a more referential shape of the C-V curve. The significant charging even at very low voltages indicates a direct hole tunneling mechanism with likely short programming times ($t_{prog} <$ ms) for higher write voltage amplitudes. A remaining difference to the unimplanted reference is mainly caused by a slight oxide swelling due to Ge insertion in SiO_2 leading to a lower C_{ox}. Such a sweep rate dependence of the C-V curves clearly indicates a fast charging behavior and should be characteristic for memories with a high density of near-interface storage nodes (NC's or traps) within the gate oxide.

Based on structural parameters and the described theoretical model the programming characteristics $\Delta V_{FB} = \mathrm{f}(V'_{gate}, \sigma, \mathrm{t})$ have been calculated and compared with experimental data $\Delta V_{FB} = \mathrm{f}(V_{prog}, t_{prog})$ in Fig. 11. For the simulations $d_{nc} = 2$ nm and $N_{nc} = 3\times10^{12}$ cm^{-2} have been used which corresponds to $R_{nc} \approx 10\%$. Thus, e.g. 2.5 holes per NC at an average cause a V_{FB}-shift of about -7V [cf. Eq. (6)]. Assuming a fixed d_{tox} without any deviation (i.e. $\sigma = 0$) the simulations result in programming characteristics with a significant stronger slope (dotted lines) compared to the

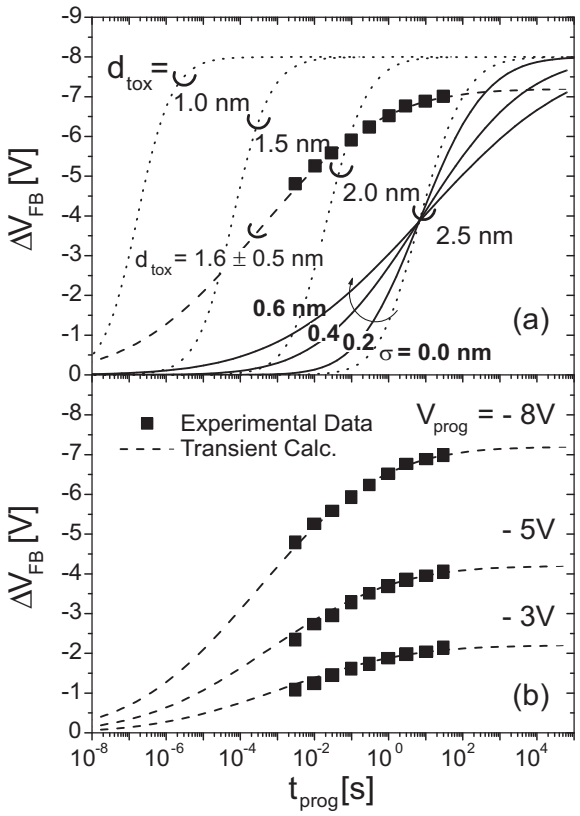

FIG. 11: (a) Comparison of the measured flatband voltage shift ΔV_{FB} (V_{prog}=-8 V) with the simulated programming characteristics for different spatial distributions of the Ge NC's: (i) 1.0 nm $\leq d_{tox} \leq$ 2.5 nm const., i.e. $\sigma = 0$ (dotted lines), and (ii) $d_{tox} = 2.5$ nm with 0.2 nm $\leq \sigma \leq$ 0.6 nm (straight lines). The dashed line indicates the best fit of the experimental result with $d_{tox}=(1.6 \pm 0.5)$ nm and V'_{gate}=-7.2 V. (b) The calculated distribution of d_{tox} holds for a series of transient programming characteristics with different programming voltages V_{prog} ($V'_{gate}/\, V_{prog}$ is -7.2 V / -8 V, -4.2 V / -5 V, and -2.2 V/-3 V).

measured data points in a semi-log plot [see Fig. 11(a)]. With increasing σ as presented in Fig. 11(a) (straight lines) the slope gets weaker. The fit of the experimental data for $d_{tox} = 1.6$ nm with $\sigma = 0.5$ nm holds for all programming voltages [Fig. 11(b)]. The charging saturates for $t_{prog} > 10$ s at $\Delta V_{FB,max} = V'_{gate}$. As in the calculation both $V_{FB,0}$ and the substrate surface potential ψ_S are neglected as constant terms, the difference V_{prog}-$\Delta V_{FB,max} \simeq$ - 0.8 V $\approx V_{FB,0}$ corresponds mainly to the work function difference ϕ_{MS} between the Al-gate and the p-Si substrate. The validity of the shape of the calculated $\Delta V_{FB}(V_{prog}, t_{prog})$ characteristic in Fig. 11 is confirmed for long programming times by our experimental data and for short write pulses by data from Hanafi *et al.*[7] obtained for Ge NC containing MOSFET devices. The simulations reveal that for a structure with near-interface Ge NC's embedded in thin gate oxides programming times of $t_{prog} < 1\,\mu$s for $|\Delta V_{FB}| \gtrsim 0.5$ V can be

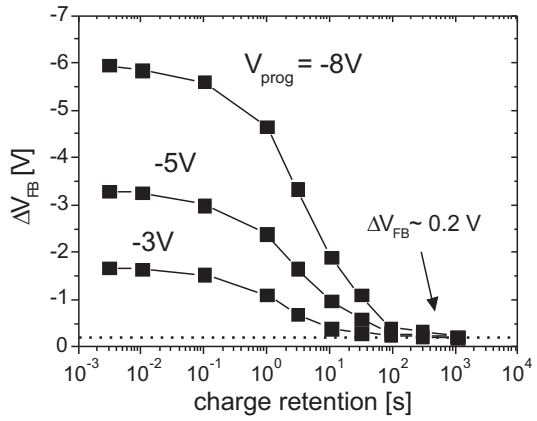

FIG. 12: Retention behavior after programming at different V_{prog} ($t_{prog} = 100\,\mathrm{ms}$).

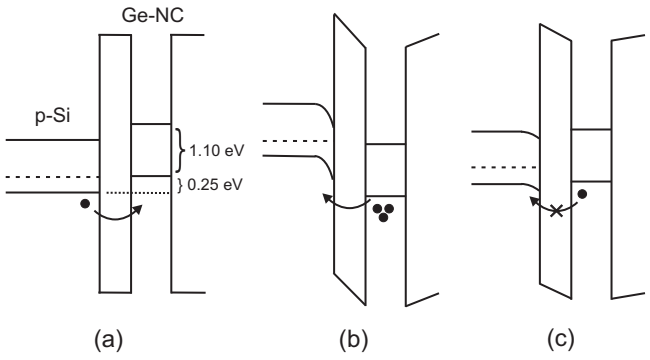

FIG. 13: Schematics of the charging and discharging process for the (a) uncharged, (b) highly charged NC and (c) stably charged state.

achieved with low programming voltages.

The results of the simulation are in remarkable agreement with the TEM results. The high sensitivity of the V_{FB}-shift to d_{tox} [cf. Fig. 11(a)] allows an extraction of structural parameters of the NC layer in the oxide by fitting the experimentally obtained charging characteristics. This offers a way to determine precisely the distribution of embedded NC's with respect to their distance to the Si/SiO_2 interface which has been shown in a separate paper.[36]

Due to the small distance to the Si substrate the charge in the Ge NC's holds just for seconds as shown in Fig. 12. Typically, the flatband voltage shift shrinks to about 20% of its initial value within 30 s after programming. But independent on the initial programming pulse height a small ΔV_{FB} of $\sim 0.2\,\mathrm{V}$ permanently remains. This shift corresponds to the valence band level difference between Ge NC's of 2 nm size ($E_g = 1.1\,\mathrm{eV}$) and the Si substrate as described before ($\sim 0.25\,\mathrm{eV}$). The remaining charge ($\approx 2.3\times10^{11}\,\mathrm{cm}^{-2}$) leads to an alignment of the valence band with a slight barrier for discharging (cf. Fig. 13). The short-time charge retention and the small remaining ΔV_{FB} reveal that the holes are captured within the valence band of the Ge NC's and not at traps at the NC's surface. In a recent paper, electron charging and trapping were attributed to a self-interstitial defect in the Ge NC but so far no similar defect level for hole trapping has been described.[37]

IV. CONCLUSION

A transient model of hole charging for gate oxides containing a NC layer close to the Si/SiO_2 interface has been developed. The close agreement between the calculated write characteristics and the experimental data clearly confirms the validity of the floating-gate-like approach with direct tunneling as the dominant charge transfer process. The investigations show that due to IBS the Ge NC's are distributed within the gate oxide with individual distance to the Si substrate. The examined structures enable short programming times and low voltages but only short data retention in the range of some seconds. Hence this memory structure shows more DRAM-like than non-volatile behavior. The applicability of the floating gate approach is restricted to a series of NC densities and sizes.

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7 Determination of the tunneling oxide thicknesses in nanocrystal memories from electrical characteristics

Determination and evolution of tunneling distances in Ge nanocrystal based memories

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A Ge nanocrystal layer embedded in a thin gate oxide was prepared by ion beam synthesis in direct-tunneling distance to the Si substrate. The write performance was investigated in metal-oxide-semiconductor capacitors by means of capacitance measurements. With the experimental data and calculations using a floating-gate-like approach the distribution of the tunneling oxide thickness d_{tox} can be determined in high precision confirmed by high-angle annular dark-field scanning transmission electron microscopy imaging. The evolution of d_{tox} during heat treatment is discussed in terms of Ostwald ripening, i.e. d_{tox} increases with annealing time.

Multidot memories are expected to replace classical floating-gate-based Flash devices in future.[1] The approach includes the nanocrystal memory[2] where preferably Si or Ge nanocrystals (NC's) embedded in thin gate oxides are used as storage nodes.[2,3] Short write/erase cycles with ultra-low power consumption and high endurance have been achieved using a direct-tunneling distance ($< 3.0\,$nm) between the NC's and the Si substrate/device channel, but this is connected to a trade-off of a short data retention (minutes or seconds).[4,5] As a consequence, the performance of such a memory is more "quasi-non-volatile" or "long refresh dynamic" than really non-volatile strongly depending on the tunneling distance. In this paper, we consider a ion-beam synthesized layer of Ge NC's in a thin SiO_2 film which is located very close ($\lesssim 2\,$nm) to the Si/SiO_2 interface. By means of capacitance-voltage (C-V) measurements at MOS (metal-oxide-semiconductor) capacitors the write performance for charging of the NC's with holes is studied. The experimental data are compared with the write characteristics calculated in a floating-gate-like approach, which enables a prediction of the flatband voltage shift for write times of μs or even below. It is shown that the measured write characteristics allow one to evaluate very precisely the distribution of the NC's distance to the Si/SiO_2 interface. The evolution of the mean distance during annealing is discussed in terms of Ostwald ripening.

A 20 nm thick gate oxide was thermally grown on <100> p-type Si ($10\,\Omega\,$cm). Ion implantation of 12 keV $^{74}Ge^+$-ions was performed at a dose of $5\times10^{15}\,cm^{-2}$ at room temperature. After standard cleaning in H_2O_2/H_2SO_4 rapid thermal annealing (RTA) was carried out at 950°C or 1050°C for 30 s in Ar. MOS capacitors ($A = 0.1\,mm^2$) were prepared by Al sputtering, photolithographic patterning and a 400°C furnace anneal in N_2 for 15 min. The Ge NC distribution in the gate oxide was characterized by scanning transmission electron microscopy (STEM) using a high-angle annular dark-field (HAADF) detector (acceptance angle about 2.8°) in a FEI Tecnai 20 FEG microscope operating at 200 kV. The write characteristic is obtained by two sequenced negative gate voltage pulses applied to the MOS capacitors, a programming (-3 V $\geq V_{prog} \geq$ -8 V with duration of 3 ms $\leq t_{prog} \leq$ 30 s) and a smaller read pulse ($|V_{read}| < |V_{prog}|$ with $t_{read} = t_{prog}$) while the C-V data $C(V_{read})$ were recorded to obtain the flatband voltage shift ΔV_{FB}.

Annealing during IBS of Ge NC's in thin SiO_2 films leads to a significant redistribution of the as-implanted Ge profile towards the Si/SiO_2 interface.[6–8] As confirmed by STEM in Fig. 1 a layer of Ge NC's forms in the oxide close to the interface. The distance between the NC's and the Si substrate, i.e. the tunneling distance d_{tox}, varies between about 0.6 and 2.5 nm.

The transient charging dQ_{nc}/dt of the Ge NC's (Q_{nc} is the effective charge density of the NC layer) is calculated in a floating-gate-like approach[4,9] according to

$$\frac{dQ_{nc}}{dt} = \left(\frac{\pi}{4}\, d_{nc}^2 N_{nc}\right) J_{DT} - J_{FN} \quad . \tag{1}$$

For negative gate voltages and low applied oxide fields ($E_{ox} < 7\,$MV/cm) the Fowler-Nordheim tunneling current (J_{FN}) of electrons from the gate can be neglected. The NC's close to the Si substrate with size d_{nc} and density N_{nc} are charged by the respective direct-tunneling hole current density J_{DT}

$$J_{DT} = A\frac{E_{tox}^2}{\phi_b}\, exp\left(-\frac{B\left[\phi_b^{3/2} - (\phi_b - |qV_{tox}|)^{3/2}\right]}{|E_{tox}|}\right) \tag{2}$$

with $A = q^3 m_0/(8\pi h m_{ox})$ and $B = 8\pi\sqrt{2m_{ox}}/(3hq)$. The tunneling barrier for holes from the emitting Si valence band is $\phi_b = 4.5\,$eV with an effective hole mass in the oxide $m_{ox} = 0.32\, m_0$, h is Planck's constant, q the elementary charge, and m_0 the free electron mass. Quantum confinement of the NC's is negligible as enough empty energy states are available for hole charging due to the relative bandgap position of Ge to Si and a quenched bandgap of the Ge NC's caused by oxygen passivation.[10] The electrical field across the tunneling oxide is given

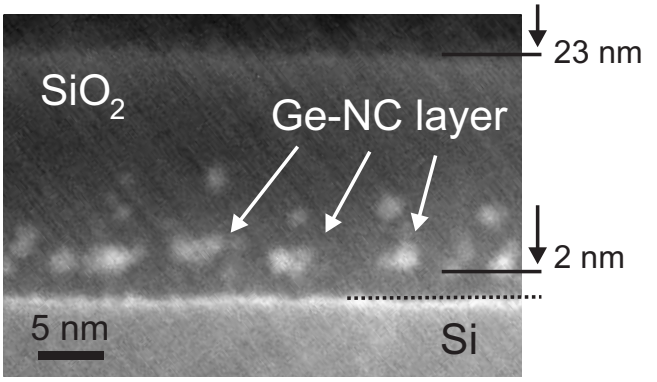

FIG. 1: HAADF STEM image of the NC's containing oxide (950°C annealing). The Ge NC's are visible by bright spots.

by $E_{tox} = V_{tox}/d_{tox}$ whereas the voltage drop across the tunneling oxide V_{tox} can be easily calculated as usual for classical floating gate memories.[4,9]

The self-organized formation of a Ge NC layer close to the Si/SiO_2 interface by IBS is a statistical process of interface-mixing, phase separation and Ge redistribution, leading to a variable distance of the NC's to the Si substrate. Thus, a normalized Gaussian distribution of d_{tox} with a standard deviation of σ is introduced. NC's far in the oxide bulk are not considered due to their long distance to the Si substrate. The calculated programming characteristics for $\Delta V_{FB}(t,\, d_{tox},\, \sigma) \sim Q_{nc}(t)$[4,9] are shown in Fig. 2 in comparison to experimental data, i.e. $\Delta V_{FB} = \mathrm{f}(V_{prog},\, t_{prog})$. The structural NC parameters are derived from the TEM image in Fig. 1 ($d_{nc} = 2\,\mathrm{nm}$ and $N_{nc} = 3{\times}10^{12}\,\mathrm{cm}^{-2}$ for the NC's vicinal to the Si substrate). Thus, a ΔV_{FB} of -7 V corresponds to 2-3 holes per NC. For a constant d_{tox} ($\sigma = 0$) the simulations [see Fig. 2(a)] result in characteristics with a stronger slope (dotted lines) compared to the measured data in a semi-log plot. With increasing σ the slope gets weaker. A fit of the measured data leads to values of $d_{tox} = 1.6\,\mathrm{nm}$ and $\sigma = 0.5\,\mathrm{nm}$, which holds for all programming voltages [Fig. 2(b)]. The charging saturates for $t_{prog} > 10\,\mathrm{s}$ for all characteristics at $\Delta V_{FB,max} = V'_{gate}$ (V'_{gate} is the gate voltage in the simulation). The constant difference to the experimental V_{prog} of $\simeq$ - 0.8 V corresponds mainly to the work function difference ϕ_{MS} between the Al-gate and the p-Si substrate. The assumed Gaussian distribution of d_{tox} in the fitting procedure is a reasonable approximation as confirmed by Fig. 3.

For a higher thermal budget, i.e. during annealing at an enhanced temperature (1050°C) or for a much longer annealing time at 950°C, d_{tox} grows and its distribution narrows to $d_{tox} = 1.75\,\mathrm{nm}$ with $\sigma = 0.40\,\mathrm{nm}$ considering d_{nc} and N_{nc} to be constant [see Fig. 2(b)]. In case that d_{tox} grows to the debit of the NC size with stable N_{nc}, one gets $d_{tox} = 1.72\,\mathrm{nm}$ for $d_{nc} = 1.8\,\mathrm{nm}$ ($\sigma = 0.40\,\mathrm{nm}$ is unaffected). Such minor changes of d_{tox} during annealing can hardly be recognized by STEM imaging which underlines the high sensitivity of the electrical characteristics. This

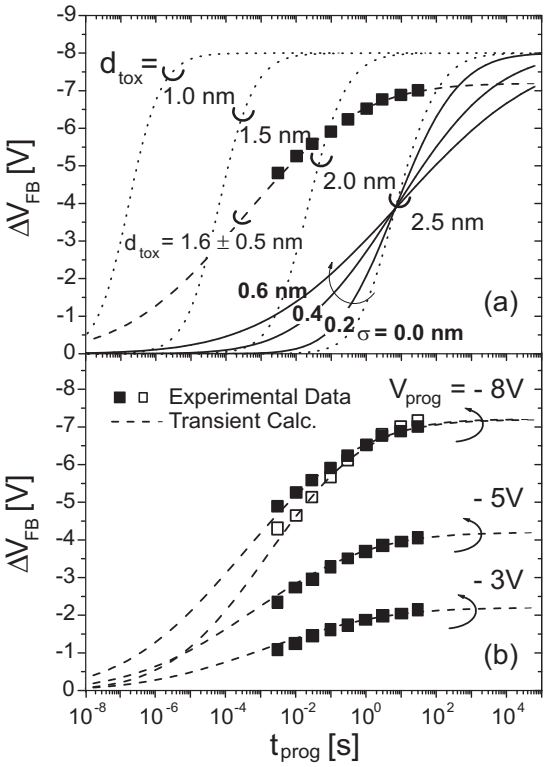

FIG. 2: (a) Comparison of the measured flatband voltage shift ΔV_{FB} (V_{prog}=-8 V) obtained for 950°C annealing (■) with the simulated programming characteristics for different spatial distributions of the Ge NC's: (i) $1.0\,\mathrm{nm} \le d_{tox} \le 2.5\,\mathrm{nm}$ const., i.e. $\sigma = 0$ (dotted lines), and (ii) $d_{tox} = 2.5\,\mathrm{nm}$ with $0.2\,\mathrm{nm} \le \sigma \le 0.6\,\mathrm{nm}$ (straight lines). The dashed line indicates the best fit of the experimental result with d_{tox}=$(1.6 \pm 0.5)\,\mathrm{nm}$ and V'_{gate}=-7.2 V. (b) The calculated distribution of d_{tox} holds for a series of transient programming characteristics with different programming voltages V_{prog}. The experimental data for the sample annealed at 1050°C are shown (□) together with a best fit for $d_{tox} = (1.75 \pm 0.4)\,\mathrm{nm}$ (V_{prog}=-8 V).

is due to the fact that $\Delta V_{FB}(t)$ is much more affected by the exponential dependence in J_{DT} ($1/E_{tox} \sim d_{tox}$) than by a change of d_{nc}.

The evolution of d_{tox} is connected to the evolution of the NC size which follows a diffusion controlled ripening process (Ostwald ripening for $t \to \infty$) considering the substrate as a crystal with infinite radius (NC size distribution has log-normal shape in the early stage of NC evolution [cf. Fig. 3]). Solving Poisson's equation for stationary diffusion fields, the solute concentration $c(\vec{r})$ leads, in an approximation for medium consisting of N sources (monopoles) with strengths Ω_i (emitted atoms from the NC surface area per second) and known location $\vec{r}_i$, to[11,12]

$$c(\vec{r}) \simeq c_u + \frac{1}{4\pi D} \sum_{i=1}^{N} \frac{\Omega_i}{|\vec{r} - \vec{r}_i|} \quad . \tag{3}$$

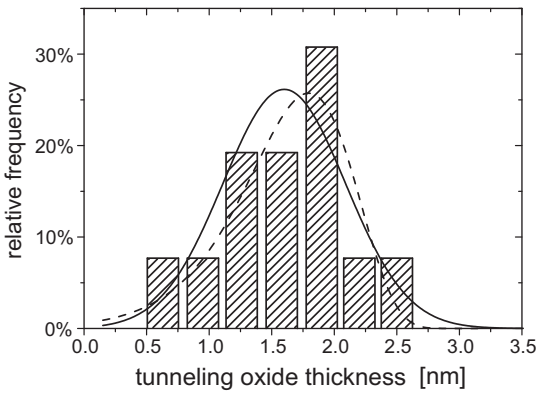

FIG. 3: Stack-histogram of d_{tox} from the NC's distribution in Fig. 1 with $d_{tox} = 1.67$ nm at an average (error ± 0.13 nm) obtained from 26 Ge NC's over 120 nm image size. The calculated Gaussian-like best-fit distribution of d_{tox} (1.6 ± 0.5 nm) corresponding to Fig. 2 (950°C) and additionally for comparison a mirrored log-normal distribution (dashed line) are shown.

The mobility of an emitted monomer in the medium depends on the diffusion coefficient D. Like in electrostatics the diffusion field caused by a single NC with radius R and source strength Ω_1 embedded in SiO_2 close to the Si/SiO_2 interface (z is the distance of the NC center to the Si substrate) can be calculated by an image source Ω_2 at distance -z within the substrate ($\Omega_2 = -\Omega_1$). At the NC surface the monomer concentration is $c(\vec{r_1}) = c_R$. A mean monomer concentration in the matrix is close to the equilibrium solubility at the substrate surface ($c_u = c_\infty$). These approximations together with the continuity equation (V_a is the atomic volume of the monomer)[12,13] expressed by

$$\Omega_1 = 4\pi D \left(\frac{c_R - c_\infty}{\frac{1}{R} - \frac{1}{2z}} \right) \quad \text{and} \quad \frac{4\pi}{V_a} R^2 \frac{dR}{dt} = -\Omega_1 \quad (4)$$

lead to the nonlinear differential equation

$$\frac{dR}{dt} = -DV_a R_c \, c_\infty \frac{1}{R^2(1 - R/2z)} \approx -\frac{d\, d_{tox}}{dt} \quad (5)$$

with respect to the linearized Gibbs-Thomson relation $c_R = c_\infty(1 + R_c/R)$ (R_c is the capillary length).[6] The evolution of the NC size by attachment or detachment of monomers is expressed by dR/dt, which is also proportional to the evolution of the tunneling oxide thickness ($d_{tox} = z - R$). Typically for Ostwald ripening, this leads to a decrease of the NC radius as

$$R(t) = \left(R_0^3 - 3\xi DV_a R_c c_\infty \, t \right)^{1/3} \approx z_0 - d_{tox}(t) \quad , \quad (6)$$

whereas the NC volume ($R(t)^3$)) dissolves in the late stage of ripening proportional to time. R_0 is the initial NC radius at an early stage ($t = 0$) after the NC's have formed. With invariant NC center position z_0 the NC's dissolve with time in the same way as the tunneling distance d_{tox} increases. The variable ξ is between $1 < \xi < 2$ within the limits of $z \approx d_{tox} \gg R$ and $z \to R$ ($d_{tox} \to 0$), respectively, i.e. the closer the NC's are located to the Si/SiO_2 interface, the faster they dissolve. In addition to the interaction with the substrate the NC's are competing with each other in-plane and above (cf. Fig. 1). This enhances the dissolution of small close NC's and stabilizes bigger more distant ones (both relative to the Si substrate). As a consequence d_{tox} grows and its distribution narrows with time which clearly confirms the experimental data and the respective model calculations.

The position of the storage nodes (here the Ge NC's) with respect to the Si substrate, i.e. the tunneling distance d_{tox}, was derived from write characteristics with high precision exceeding TEM imaging capability. A close agreement between experimental data and calculations based on a modified floating gate approach confirms direct-tunneling as the dominant charge transfer process. Possibly occurring trap-assisted tunneling would be interpreted as a shortened d_{tox}. The general applicability of the model depends on the relevance of e.g. quantum confinement effects which is connected to NC material, density and size. A higher thermal budget during IBS leads to an increase of d_{tox} which is explained, in agreement with the theory of Ostwald ripening, due to a dissolution of small NC's close to the Si substrate. This confirms the validity of the model calculations according to experimental data with respect to multidot memory device performance adjustment.

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8 Leakage current-voltage characteristics of nanocrystal containing thin gate oxides

Current-voltage characteristics of metal-oxide-semiconductor devices containing Ge or Si nanocrystals in thin gate oxides

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Current-voltage characteristics were measured, electrically modeled, and calculated for gate oxides which contain nanocrystals (NC's) in different distributions, sizes and densities. Ge and Si NC's were synthesized embedded in separate thin SiO_2 layers by ion implantation at different fluences and subsequent annealing. It was found that the currents through the NC containing thin gate oxides are strongly related to the NC's location and are not driven by ion implantation induced oxide defects. Charging of the NC's determines the internal electrical fields which is confirmed by simultaneous current and capacitance measurements. Depending on the implanted fluence the Ge NC's were mainly detected in the oxide center or close to the Si/SiO_2 interface. The Si NC's were fabricated in the oxide center sandwiched between two oxide regions denuded of NC's. The processes of Si NC formation, growth and dissolution are discussed by means of kinetic lattice Monte Carlo simulations.

I. INTRODUCTION

Due to a potential application for memory devices,[1] (mainly Si or Ge) nanocrystals (NC's) embedded typically in $\leq 30\,\mathrm{nm}$ thin oxide layers are intensively studied in the past decade,[2–5] especially for the case of a short ($< 5\,\mathrm{nm}$) tunneling distance between the NC's and the Si substrate. Such devices still suffer mainly from a weak data retention (less than hours) since for real non-volatility more than 10 years are required. Tunneling barrier and work function engineering are under discussion to improve the charge storage performance using layered barriers[6] with alternative oxide materials like HfO_2 or Al_2O_3 and/or metal (e.g. Au, Pt, W) NC's,[7] respectively, and also double stacked storage nodes.[8] Although attention is focused on the programming and storage behavior, current-voltage (I-V) characteristics are of great interest with respect to the oxide stability and the role of leakage currents during write and erase operations. Such characteristics involve all charging and de-charging mechanisms like the injection of holes and electrons from the Si substrate or gate electrode as well as their in- and ejection to/from the tiny semiconductor NC's. Different charge transfer mechanisms were discussed considering charging (or non-charging) currents in memory structures containing a floating gate,[9] a Si_3N_4 trapping layer[10] or Si NC's[11] embedded in the gate oxide. For Si implanted oxides charge trapping is supposed to be dominant[12] neglecting the final spatial distribution of charge conducting sites like the formation of NC's. More reliable, a transient electrical model was developed to describe programming characteristics of Ge NC's embedded in thin gate oxides.[13] Enabled by this model it was possible to determine individual tunneling distances (tunneling oxide thickness) between the Si substrate and the NC's from electrical capacitance-voltage (C-V) measurements.[14] Here, this transient model[13] is extended to evaluate the I-V characteristics for 20 nm thin gate oxides with embedded Ge or Si NC's prepared by ion beam synthesis (IBS).[2,15–18] Despite a similar initial profile of Ge and Si impurities in SiO_2 after the ion implantation, the final distributions of the NC's are quite different. Since after Ge^+ implantation a narrow layer of Ge NC's was obtained in vicinity to the Si/SiO_2 interface during annealing (a favored configuration for nanocrystal memory devices),[19] a broad layer of Si NC's formed in the oxide center sandwiched between two oxide layers in case of Si implantation. The determination and localization of the embedded NC's is one of the particular challenges to give a reliable electrical model to explain the charge transfer characteristics of such oxides. These structural data were derived from transmission electron micrographs and discussed by means of kinetic lattice Monte Carlo simulations in order to understand the role of a close Si substrate for the Si NC formation.[20,21] Respective I-V characteristics were calculated based on a detailed electrical model with significant agreements to measurements obtained on metal-oxide-semiconductor (MOS) capacitors with Si and Ge NC's embedded in the gate oxides.

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TABLE I: Low (LD) and high fluence (HD) ion implantation and annealing parameters.

ion	energy [keV]	LD [cm^{-2}]	HD [cm^{-2}]	annealing
$^{74}Ge^{+}$	12	5×10^{15}	1.5×10^{16}	950°C/1050°C, 30 s
$^{28}Si^{+}$	6	7×10^{15}	2.0×10^{16}	1050°C, 30 s/ 120 s

II. EXPERIMENTAL DETAILS

$^{74}Ge^{+}$ or $^{28}Si^{+}$ ions were implanted with different energies and fluences (summarized in Tab. I) into 20 nm thick gate oxides which were thermally grown on <100> p-Si substrates with a resistivity of 10 Ω cm. After standard cleaning in H_2O_2/H_2SO_4 rapid thermal annealing (RTA) was carried out between 950 and 1050°C for 30 or 120 s in Ar atmosphere. MOS capacitors were prepared in 3×10^{-4} cm^2 (Ge) and 1×10^{-3} cm^2 (Si) size by Al sputtering, photolithographic patterning and furnace annealing at 400°C for 15 min in N_2. The NC's distribution in the gate oxide is characterized by bright and high angle annular dark field (HAADF) high-resolution (HR-) transmission electron microscopy (TEM) using a Philips CM300 microscope operating at 300 kV. Energy-filtered (EF-)TEM investigations were performed to detect tiny Si NCs using a Gatan image filter in a 200 keV FEI Tecnai 20 FEG microscope with a 5 eV window and 18 eV onset at a collection angle of 15 mrad. The Ge, Si and O profiles were characterized by Rutherford backscattering spectrometry (RBS) using 1.7 MeV He^{+} ions; the incident angle was set to 70° to improve the depth resolution (scattering angle is 170°). The current-voltage (I-V) characteristic of the MOS capacitors were obtained by a Keithley 237 voltage source. A Keithley 590 capacitance-voltage (C-V) analyzer working at 100 kHz and a Keithley 617 electrometer were combined (using a Keithley 590-1 coupling box) to provide simultaneous capacitance and current acquisition during a stepwise voltage sweep (see Fig. 1).

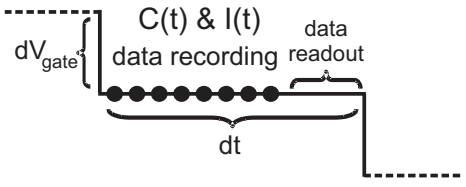

FIG. 1: Sequence of the simultaneous capacitance and current measurements during a stepwise gate voltage sweep performed with dV_{gate} = -0.5 V. During a time period dt = 7 s at constant gate voltage, capacitance and current data are recorded in intervals of 300 ms followed by a data readout from the measurement instruments.

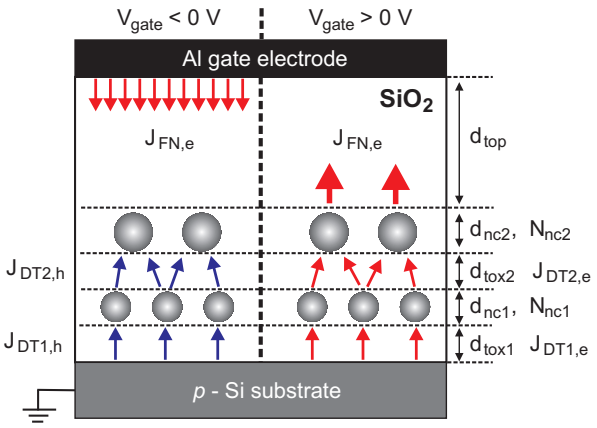

FIG. 2: (Color online) Schematic of a NC containing gate oxide with two embedded NC layers of different NC size and density. The flux of electrons and holes is indicated by colored arrows (red and blue, respectively) depending on the V_{gate} polarity.

III. MODELING OF I-V CHARACTERISTICS FOR GATE OXIDES WITH EMBEDDED NC'S

A MOS structure is electrically modeled for both gate voltage polarities as shown in Fig. 2 with two parallel NC layers embedded in a gate oxide with NC densities $N_{nc1,2}$ and same NC sizes $d_{nc1,2}$ within each layer. The NC layers are separated to the Si substrate and to each other by the tunneling oxides d_{tox1} and d_{tox2}, respectively, and to the gate electrode by the top-oxide d_{top}. Tunneling of electrons or holes from Si electrodes through oxides of different size can generally be described by the equations[22–24]

$$J_{DT-FN,c} = \frac{q^3(m_{si,c}/m_{ox,c})}{8\pi h\phi_{b,c}} E_{tox}^2 \Theta_{ox,c} \quad \text{with} \qquad (1)$$

$$\Theta_{ox,c} = exp\left(-\frac{8\pi\sqrt{2m_{ox,c}}\left[\phi_{b,c}^{3/2} - [\Gamma^{3/2} \times H(\Gamma)]\right]}{3hq|E_{tox}|}\right),$$

$$\Gamma = (\phi_{b,c} - |qV_{tox}|) \quad \text{and} \quad c = e|h$$

whereas the Heaviside function $H(x)$ enables a continuous transition between direct (DT) [$H(x)=1$ for $\Gamma>0$, i.e. $J_{DT-FN} = J_{DT}$] and Fowler-Nordheim (FN) tunneling [$H(x)=0$ for $\Gamma\leq 0$, i.e. $J_{DT-FN} = J_{FN}$]. Θ_{ox} is the transmission probability for charge carriers through the respective oxide according to a parabolic dispersion relation with respect to Wentzel-Kramers-Brillouin (WKB) approximation.[10,22,24,25] h is Planck's constant, q the magnitude of electron charge, and m_0 the free electron mass. Depending on the gate voltage polarity, holes ($V_{gate}<0$ V) or electrons ($V_{gate}>0$ V) are injected from the accumulated or inverted p-Si substrate toward the NC's. $V_{tox1,2}$ and $E_{tox1,2} = V_{tox1,2}/\, d_{tox1,2}$ are the voltage drop and the electric field across the tunneling oxides, respectively; the same holds for the top-oxide voltage drop V_{top} with $E_{top} = V_{top}/\, d_{top}$. Values for the tun-

TABLE II: Summarized parameter for the tunneling barriers ϕ_b and the effective hole and electron masses for direct (DT) and Fowler-Nordheim (FN) tunneling.

	emitting electrode	tunneling barrier	effective masses
FN	Si (inv.)	$\phi_{b,e} = 2.9\,\mathrm{eV}$ [22]	$m_{ox,e} = 0.5\,m_0$ [22] $m_{si,e} \approx m_0$ [24]
	Al	$\phi_{b,e} = 3.2\,\mathrm{eV}$ [26]	$m_{ox,e} = 0.5\,m_0$ [22] $m_{al,e} = m_0$ [22]
DT	Si (acc.)	$\phi_{b,h} = 4.5\,\mathrm{eV}$ [13,25]	$m_{ox,h} = 0.32\,m_0$ [13,25] $m_{si,h} \approx m_0$ [13]
	Si (inv.)	$\phi_{b,e} = 2.9\,\mathrm{eV}$	$m_{ox,e} = 0.42\,m_0$ [a] $m_{si,e} \approx m_0$ [24]
DT	Ge NC	$\phi_b = \mathrm{f}(d_{nc})$ [b]	$m_{ge,h} = 0.324\,m_0$ [26] $m_{ge,e} = 1.64\,m_0$ [26]

[a] see Fig. 3
[b] see Tab. IV

neling barrier height ϕ_b and the effective hole or electron masses in the Si substrate m_{si} and in the oxide m_{ox} are summarized in Tab. II (h or e indicates holes or electrons, respectively). m_{si} has to be replaced by m_{al} or m_{ge} if the charges are ejected from the Al-gate electrode or the Ge NC's, respectively. For the DT regime ϕ_b and m_{ox} are verified in Fig. 3 by means of recently published current-voltage data using Eq. (1) with $H(x) = 1$. In order to validate ϕ_b and m_{ox} for FN tunneling of electrons, reference data (unimplanted oxides) are fitted in Figs. 9, 10, and 19 (curves C) using Eq. (1) with $H(x) = 0$ and a gate oxide thickness of $d_{ox} = 20.5\,\mathrm{nm}$ (or 20.7 nm, respectively).

The total current density J_{tot} has three different components describing the charging/discharging of the gate oxide from the electrodes. The first layer of NC's is charged from the substrate side by $J_{DT1} = \mathrm{f}(V_{tox1},\, d_{tox1})$ [see Eq.(1) in the DT regime]. $J_{FN,e}$ describes the charge exchange with the gate electrode through the top oxide by a FN mechanism if $d_{top} > 5\,\mathrm{nm}$. Here, the current through the oxide J_{ox} besides the NC's is negligible in most cases.

$$J_{tot} = R_{nc1}\,J_{DT1} + J_{FN,e} + (1 - R_{nc1})\,J_{ox} \approx R_{nc1}\,J_{DT1} + J_{FN,e} \qquad (2)$$

The relative portion of area covered by NC's R_{nc} (surface coverage ratio), given by the ratio of the square NC surfaces A_{nc} to the total capacitor area A_{tot}, is a key factor of memory programming characteristics and not only the dot density N_{nc}.[32]

$$R_{nc} = A_{nc}/A_{tot} = \frac{\pi}{4}\,d_{nc}^2 N_{nc} \qquad (3)$$

The charge density on the first NC layer Q_{nc1} determines the current density $J_{DT2} = qnf\,T$ from the first NC layer to the second.[25,33] There, T is the oxide transparency,

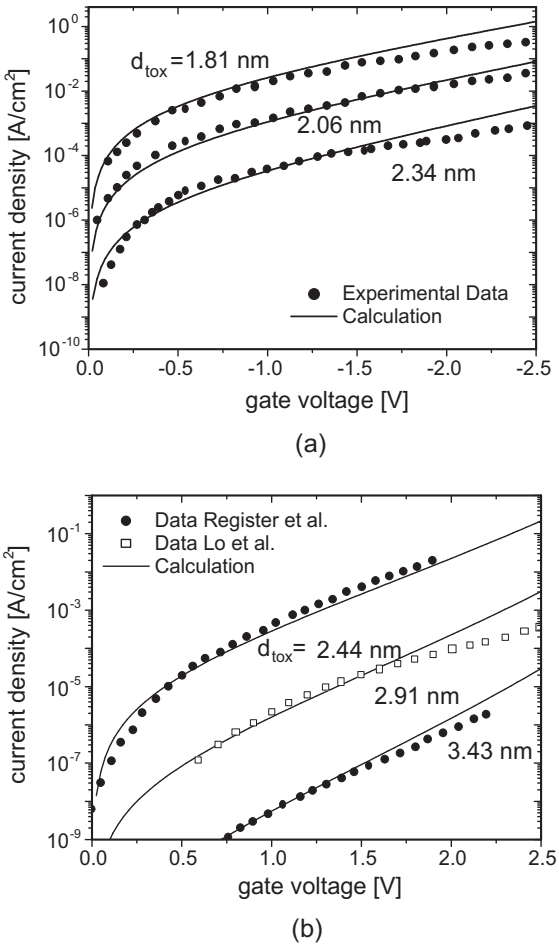

FIG. 3: Calculated DT currents of holes (a) and electrons (b) according to Eq. (1) with $H(x) = 1$ in comparison to experimental data with the same oxide thicknesses (hole current: Refs. 27, 28, and 29; electron current: Refs. 30 and 31). The best fit is achieved for $\phi_{b,h} = 4.5\,\mathrm{eV}$ with $m_{ox,h} = 0.32\,m_0$ [25] (a) and $\phi_{b,e} = 2.9\,\mathrm{eV}$ with $m_{ox,e} = 0.42\,m_0$ (b) ($m_{si,e} = 0.916\,m_0 \approx\ m_0 \approx m_{si,h}$ [13,24]).

f the impact frequency against the barrier, and n is the density of charge carriers available for tunneling, thus $qn = Q_{nc1}$. With $\varepsilon_{ox}\varepsilon_0 E_{tox2} = Q_{nc1}$ Eq. (1) changes with $H(x) = 1$ (DT is dominant with $d_{tox2} \approx 2\,\mathrm{nm}$) to

$$J_{DT2} = \frac{q^3 (m_{nc}/m_{ox})}{8\pi h \phi_b} \frac{Q_{nc1}}{\varepsilon_{ox}\varepsilon_0} |E_{tox2}|\,\Theta_{tox2} \qquad (4)$$

with $\Theta_{tox2} = \mathrm{f}(V_{tox2},\, d_{tox2})$. In the same way we find for the current from layer 2 to the gate electrode

$$J_{FN,e} = \frac{q^3 (m_{nc}/m_{ox})}{8\pi h \phi_b} \frac{Q_{top}}{\varepsilon_{ox}\varepsilon_0} |E_{top}|\,\Theta_{top}\,. \qquad (5)$$

m_{nc} is the effective mass of charge carriers in the NC's. The effective mass of holes in Ge NC's $m_{ge,h}$ is set to its bulk value as a sum of the effective masses of light and heavy holes[27] $m_{nc,h} = m_{ge,h} = m_{ge,lh} + m_{ge,hh} = (0.044 + 0.28)\,m_0 = 0.324\,m_0$ [26]; for electrons $m_{nc,e} = m_{ge,e} = 1.64\,m_0$.[26]

The current through the gate oxide with embedded NC's is calculated as a function of sweep time. Thus, the actual NC charge areal density Q_{nc} on each layer is iteratively calculated using

$$\begin{aligned} Q_{nc1,2}(t_{i+1}) &= Q_{nc1,2}(t_i) + dQ_{nc1,2}(t_i) \quad , \qquad (6)\\ dQ_{nc1}(t_i) &= [R_{nc1}J_{DT1}(t_i) - R_{nc2}J_{DT2}(t_i)]\Delta t \\ \text{and} \quad dQ_{nc2}(t_i) &= [R_{nc1}J_{DT2}(t_i) - J_{FN,e}]\Delta t \; . \end{aligned}$$

The equations hold for small time increments Δt so that the potentials within the gate oxide do not change significantly between the time steps t_i and t_{i+1}. For the case $V_{gate} \ll 0\,\mathrm{V}$ a radiative (e.g. band to band with light emission) or non-radiative recombination (e.g. Auger) of electron hole pairs in the NC's of layer two (Q_{nc2}) is assumed. Thus,

$$\begin{aligned} V_{tox1} &= \frac{d_{tox1}}{d_{tot}}\left[V'_{gate} + \frac{Q_{nc1}}{\varepsilon_{ox}/(d_{k2}+d_{top})} + \frac{Q_{nc2}}{\varepsilon_{ox}/d_{top}}\right] ,\\ V_{top} &= \frac{d_{top}}{d_{tot}}\left[V'_{gate} - \frac{Q_{nc1}}{\varepsilon_{ox}/d_{k1}} - \frac{Q_{nc2}}{\varepsilon_{ox}/(d_{tot}-d_{top})}\right] , \quad (7)\\ \text{and} \quad V_{tox2} &= \frac{d_{tox2}}{d_{k2}}\left[V'_{gate} - \frac{d_{k1}}{d_{tox1}}V_{tox1} - V_{top}\right] \end{aligned}$$

$$\text{with} \quad d_{tot} = d_{k1} + d_{k2} + d_{top} \, ,$$

$$d_{k1} = d_{tox1} + \frac{\varepsilon_{ox}}{\varepsilon_{nc}}\, d_{nc1} \quad \text{and} \quad d_{k2} = d_{tox2} + \frac{\varepsilon_{ox}}{\varepsilon_{nc}}\, d_{nc2}$$

assuming for simplicity that the charges in the NC's (electrons or holes) are located at the NC/SiO_2 interface towards the gate electrode. As shown by electron density calculations this is a reasonable approximation for biased tiny spherical Si nanodots embedded in SiO_2.[34] ε_{ox} and ε_{nc} are the dielectric constants for SiO_2 and the NC material (bulk value), respectively.

$$V'_{gate} = V_{gate} - V_x(t_0) \qquad (8)$$

$V_x(t_0)$ is the initial flatband (V_{fb}) or threshold (V_t) voltage for the uncharged state disregarding the exact Si substrate surface potential.

IV. Ge NANOCRYSTAL CONTAINING GATE OXIDES

A. Structural data for Ge implanted gate oxides

After ion implantation (Fig. 4) the peak concentration of Ge in the oxide reaches of about 7 (LD) or 16 (HD) at.%. Ion beam synthesis of Ge nanocrystals in thin SiO_2 is associated with a significant redistribution (and also a partial loss) of the implanted Ge as shown in Fig. 5; its physical origin has been described elsewhere.[19] Depending on the implantation fluence, a layer of tiny Ge NC's ($d_{nc} = 2\,\mathrm{nm}$) is formed in vicinity to the Si/SiO_2 interface or a layer of bigger ones ($d_{nc} = 4\,\mathrm{nm}$) in the oxide

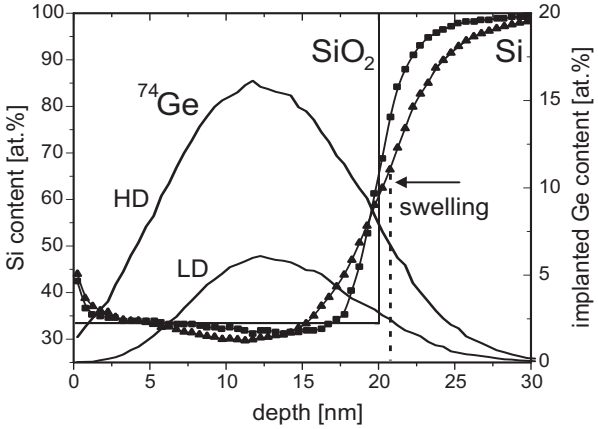

FIG. 4: Si content (left ordinate) and Ge profiles (right ordinate) after Ge ion implantation into 20 nm SiO_2. The Si content is obtained from TRIDYN calculations[35] [LD (■) and HD (▲)] taking sputtering and swelling effects into account (dashed line). The box shape profile indicates the Si concentration before implantation. The implanted Ge profiles (right ordinate) are given by straight lines.

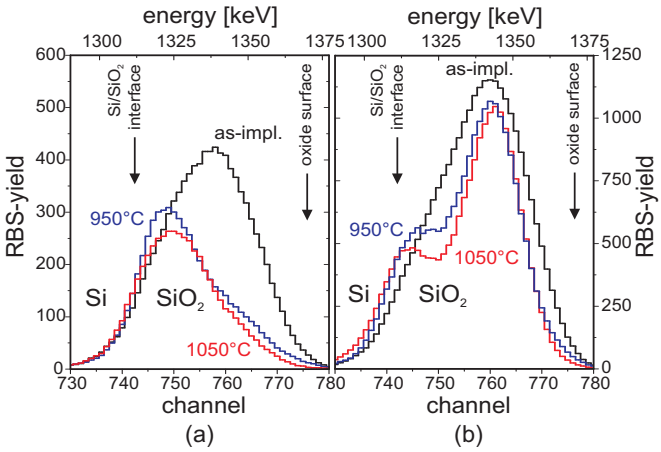

FIG. 5: (Color online) Ge profiles as obtained by RBS for the lower and the higher fluence implanted samples in (a) and (b), respectively. With annealing about 40% (LD) or 25% (HD) of the initially implanted Ge amount disappeared. The data are smoothed for clarity averaging five adjacent.

center as shown in Figs. 6 and 7, respectively. In both cases during annealing a top-oxide region forms without Ge NC's. In order to transfer these structures into an one-dimensional electrical model, the statistical distribution of Ge NC's is simplified into two parallel NC layers as shown schematically in Fig. 2. The thicknesses of the oxides and NC layers are summarized in Tab. III as deduced from the TEM micrographs in Figs. 6 and 7. Ideal DT charge conduction is assumed from layer to layer, although probably also trap-assisted tunneling mechanisms may be involved in the real system. Although hardly detectable in Fig. 7, a high concentration of Ge precipitates enables an effective charge exchange between the main

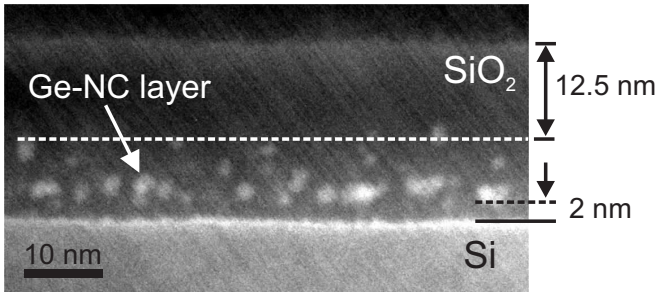

FIG. 6: HAADF STEM micrograph after Ge implantation, LD in 20 nm SiO_2 and annealing at 950°C for 30 s. Bright spots indicate Ge NC's of about 2 nm size arranged in a layer close to the Si/SiO_2 interface in a very high density and also a few NC's distributed close to these toward the oxide bulk.

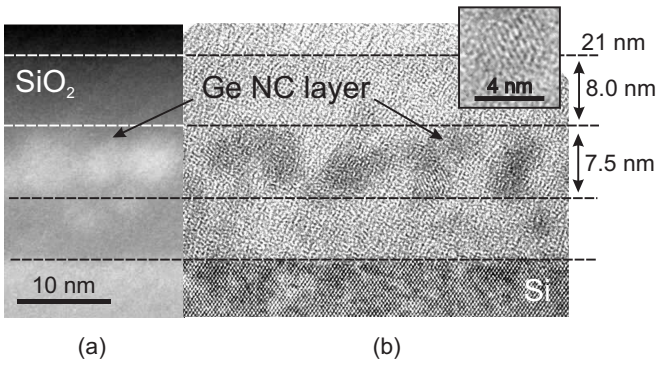

FIG. 7: Merged TEM micrographs obtained at HAADF (a) and high resolution bright field (b) conditions for the same high fluence Ge implanted sample (HD) annealed at 950°C for 30 s. A high density of Ge NC's in 4 nm size are detected in the oxide center and also smaller ones (or just precipitates) between this NC layer and the Si substrate.

NC layer and the Si substrate similar to an intermediate layer of tiny NC's. The d_{nc} and N_{nc} values for both layers are deduced from the TEM micrographs to calculate R_{nc} (see Tab. IV). The evaluation of the band gap energy of tiny Ge NC's in Tab. IV and thus of the tunneling barriers ϕ_b for electron and holes emission from the Ge NC's needs a more detailed discussion. Due to quantum confinement the band gap energy of tiny NC's increases with decreasing NC size. This effect is significantly quenched considering oxygen passivated NC's as in the present case of Ge NC's embedded in SiO_2.[36] As shown in Fig. 8, Ge NC's of 2 nm size have a band gap energy of about 1.1 eV, which leads to tunneling barrier heights of $\phi_{b,e} \approx 2.9$ eV and $\phi_{b,h} \approx 4.5$ eV with respect to SiO_2 using the Ge bulk electron affinity ($\chi = 4.0$ eV) and the bulk energy gap of $E_g = 0.67$ eV[26] as a reference (see Ref. 13 for details).

TABLE III: Structural parameters used in the calculation of the current-voltage characteristics (distances in nm). Letters A-E refer to the simulated *I-V* curves in Figs. 9 and 10.

fluence	curve	d_{tox1}	d_{nc1}	d_{tox2}	d_{nc2}	d_{top}	d_{ox}
LD	A/E	2.0	2.0	2.3	2.0	12.5	20.8
	B	2.0	2.0	-	-	16.8	20.8
	C	-	-	-	-	-	20.5
	D	-	-	-	-	-	16.8
HD	A/E	2.0	2.0	2.0	7.5	8.0	21.5
	B	2.0	2.0	2.0	6.0	9.5	21.5
	C	-	-	-	-	-	20.5
	D	-	-	-	-	-	8.0

TABLE IV: Ge NC sizes d_{nc} and densities N_{nc} as deduced from the STEM images in Figs. 6 and 7 in a two layer approximation together with the relative NC capacitor area ratios R_{nc} and tunneling barrier heights ϕ_b obtained using Eq. (3) and Fig. 8, respectively. E_g is the Ge NC band gap energy.

fluence	layer	d_{nc} [nm]	N_{nc} [cm^{-2}]	R_{nc}	E_g [eV]	$\phi_{b,e}$ [eV]	$\phi_{b,h}$ [eV]
LD	1	2.0	3×10^{12}	0.1	1.1	2.9	4.5
	2	2.0	3×10^{11}	0.01	1.1	2.9	4.5
HD	1	2.0	1×10^{12}	0.03	1.1	2.9	4.5
	2	4.0	5×10^{12}	0.6	0.9	3.0	4.6

B. Current-voltage (*I-V*) characteristics

In Figs. 9 and 10 measured *I-V* characteristics for both gate voltage polarities are shown for the virgin (reference) and Ge implanted oxides superimposed with the calculation results. For negative gate voltages the minority carrier generation in the Si substrate is stimulated by light exposure. Nevertheless, the generation rate limits

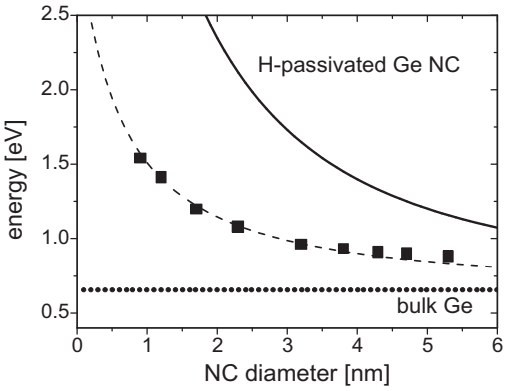

FIG. 8: Calculated quantum confinement of H-passivated Ge NC's after *Niquet et al.*[37] (straight line) as function of NC size in comparison to measured photoluminescence (PL) data[38] for oxygen passivated Ge NC's (■).

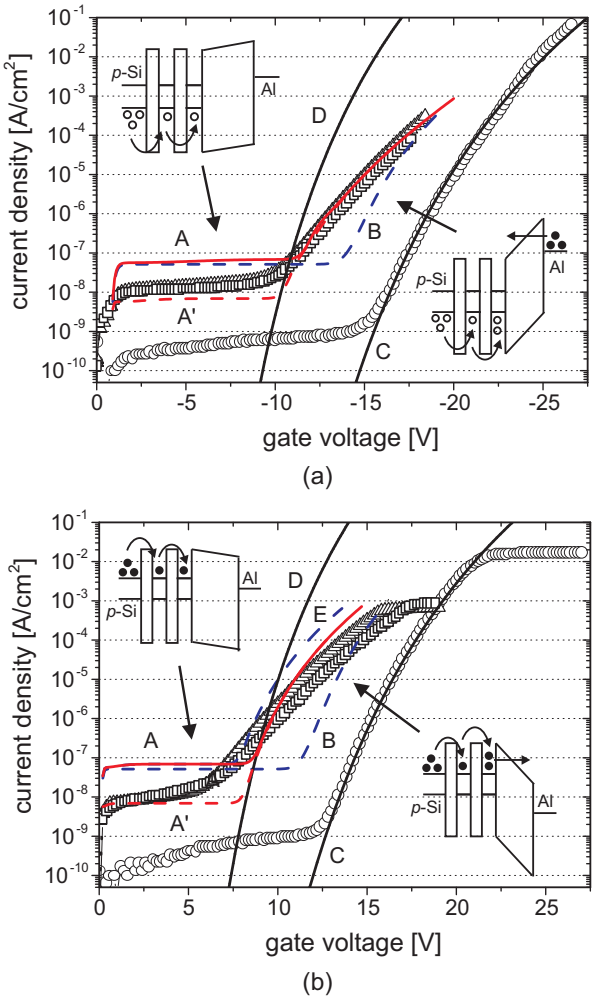

FIG. 9: (Color online) I-V characteristics for the Ge, LD implanted oxides annealed at 950°C (□) and 1050°C (△) and the unimplanted reference (◯) for comparison, all for each gate voltage polarities in (a) and (b), respectively. The red and blue lines (curves A, B, and E) reflect the results of the model calculations related to Ge NC containing oxides. The straight black lines (curves C and D) show the calculated FN currents [using Eq. (1)] for pure oxides of different thicknesses without NC's. Used structural and electrical parameters are summarized in Tab. II, III, and IV. Sweep rates are 0.25 V/s for the measurements and calculations, reduced to 0.025 V/s for calculations of curves A' (V_{fb} = - 0.8 V and V_t = 0.1 V for all calculations). For curves E the electron barrier height is set to $\phi_{b,e}$ = 2.7 eV which corresponds to a Ge NC size of about 1 nm for NC layer 2. The insets reflect schematically the charge transfer processes for the respective current components.

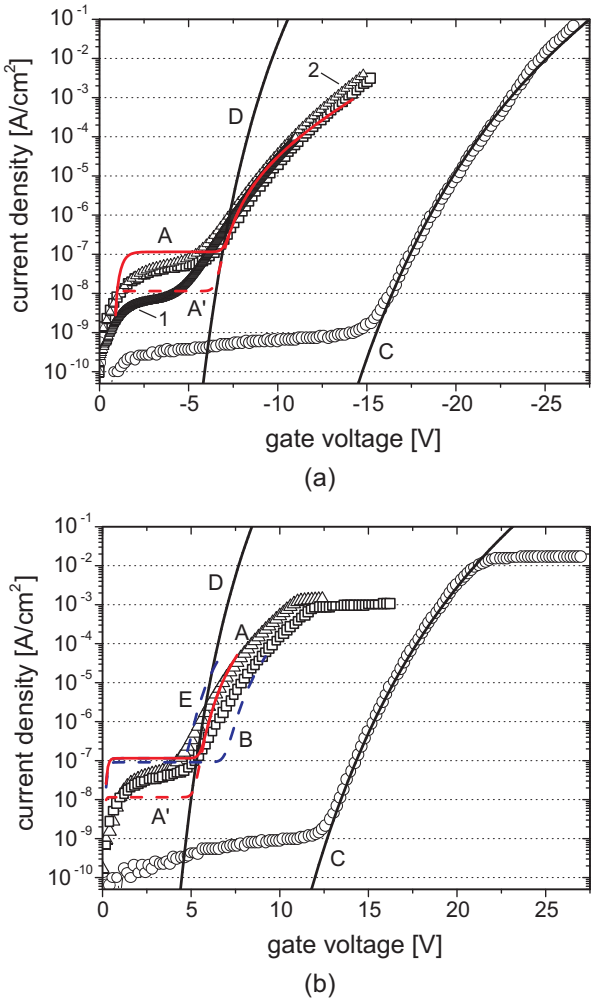

FIG. 10: (Color online) Measured and calculated I-V characteristics for the Ge, HD implanted samples (for details see caption of Fig. 9). In (a) data for different sweep rates are shown, for 0.025 V/s (1 and A') and 0.25 V/s (2 and A).

the number of electrons available for tunneling leading to a saturation of the tunneling currents in Figs. 9/10(b).

Especially in Figs. 9/10(a) the calculated I-V characteristics (labeled as A) show significant agreements with the measured data (symbols). As schematically shown in the insets of Fig. 9(a), at negative V_{gate} the Ge NC's in both layers are positively charged by DT of holes from the p-Si substrate. As a consequence V_{gate} drops mainly across d_{top} where finally electrons are injected from the metal gate side by FN tunneling indicated by the rapidly rising current at V_{gate} = -10 V or -6 V in Figs. 9(a) and 10(a), respectively. These electrons get trapped at the Ge NC's and compensate the positive charges e.g. by radiative recombination of electron-hole pairs. Accordingly, for positive V_{gate} [Fig. 9/10(b)] the NC's are charged by electrons which are emitted at high gate voltages from individual NC's toward the gate electrode (high current region). On the contrary to homogenous emission of electrons from an equal potential metal gate electrode ($V_{gate} < 0$ V), in this case the curved surfaces of the tiny NC's cause an inhomogeneous emission due to enhanced electrical fields near the NC/top-oxide interface.[39] This might explain the slight differences between the calculated characteristic and the measured data in Figs. 9/10(b). Individually deviating NC sizes with different $\phi_{b,e}$ have to be taken into account (curves E for

smaller NC's) as well as the emission of electrons at high gate voltages from NC's which are located deeper in the oxide (curves B for a single NC layer). However, the high current part of the *I-V* characteristics is related to the FN emission of electrons from the gate electrode or from the NC's side across d_{top} depending on the V_{gate} polarity. Thus, the onset for this FN current coincidences with calculated characteristics for FN tunneling through a pure thermally grown oxide (curves D in Figs. 9 and 10) with a thickness similar to top-oxide thicknesses d_{top} as deduced from the TEM of the Ge NC containing oxides (see Tab. III). Hole FN tunneling can be neglected due to the high barrier towards SiO_2. The annealing temperature has only a marginal influence on the shape of the *I-V* characteristics.

For both polarities the measured *I-V* characteristics reveal in the low voltage range [e.g. -10 V < V_{gate} < 6 V in Fig. 10(a)] a nearly constant current which is for the NC containing gate oxides about 100 times higher than for the unimplanted oxides. This current level decreases proportional to the sweep rate, in both, simulation (labeled as 1 and 2) and measurement (A and A') in Fig. 10(b). The FN tunneling current is not affected by the sweep rate. Both, for the unimplanted reference and for the implanted oxide this nearly constant current can be described by a displacement current which is $J_{dpl} = C_{ox}\,(\mathrm{d}V_{gate}/\mathrm{d}t)$ for the reference. $C_{ox} = \varepsilon_{ox}/d_{ox}$ is the oxide capacitance and $\mathrm{d}V_{gate}/\mathrm{d}t$ the sweep rate. The measured J_{dpl} value for the unimplanted reference is about two orders lower than the theoretical value of $J_{dpl} = 4.2\times10^{-8}$ A/cm^2 because V_{gate} is not sweeped constantly but stepwise. Thus, J_{dpl} decreases exponentially during the delay time after each voltage step of 0.5 V (see Fig. 1) which is performed to achieve a higher current resolution. For the NC containing oxides J_{dpl} corresponds to the non-equilibrium charging current of the top-oxide through $d_{tox1,2}$. The variable resistance of the tunneling oxides defines the time constant of charging and also of the decay of J_{dpl} after each voltage step. A higher low voltage current for the Ge, HD implanted compared to the Ge, LD implanted sample reflects the different tunneling or charging resistances and/or mechanisms. In the latter case a well-defined NC layer with a higher NC density is charged, whereas in the first case (HD) the current is probably more related to a trapping-like conduction.

C. Simultaneous *C-V*/*I-V* measurements

C-V characteristics were obtained to reveal the charging behavior of the Ge NC containing gate oxides (see Fig. 11). Already very small sweep amplitudes of ±2.5 V create a significant *C-V* hysteresis. Holes as well as electrons are rapidly stored at the NC's in similar amount where the *C-V* characteristics shift continuously with the applied voltage (see Ref. 13 for details). Thus, the characteristics for the Ge, LD implanted oxide in Fig. 11(a) do not reach the expected maximum capacitance value of

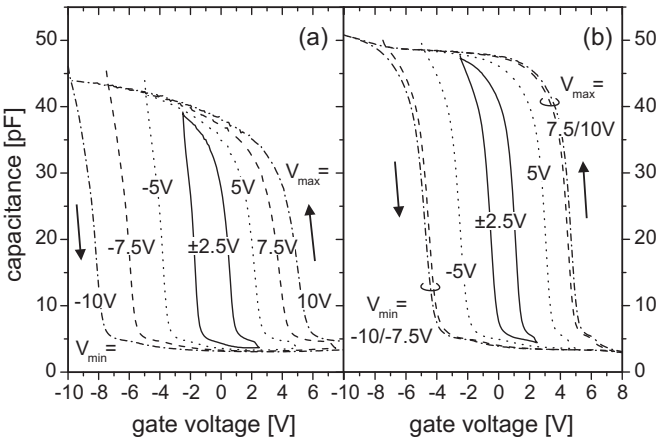

FIG. 11: *C-V* hysteresis characteristics for Ge implanted gate oxides, LD (a) and HD (b), both annealed at 950 °C for 30 s. Sweep direction is $V_{min} \rightarrow V_{max} \rightarrow V_{min}$ for ± 2.5 V/± 5 V/± 7.5 V/± 10 V amplitudes.

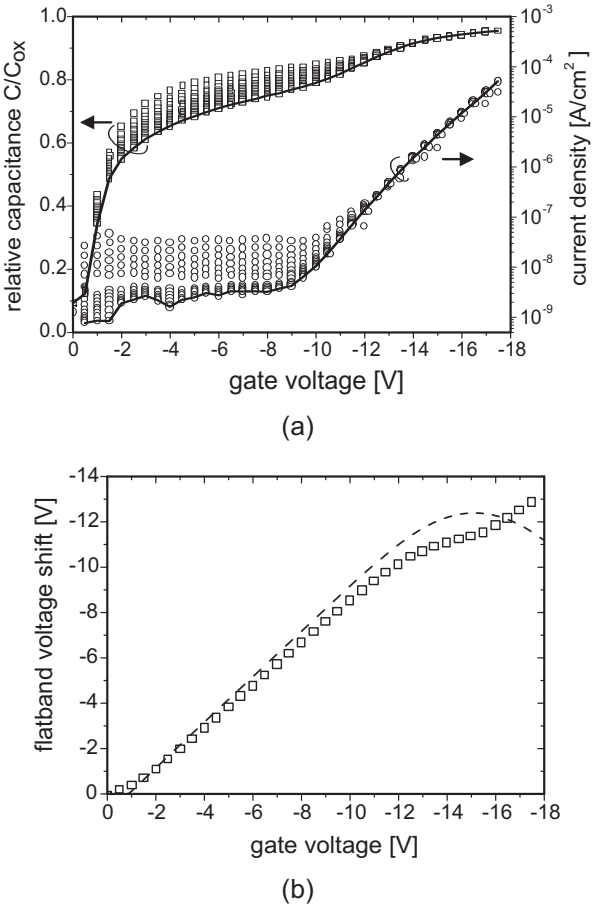

FIG. 12: (a) *C-V* and *I-V* data simultaneously recorded as a function of sweep time for the Ge, LD implanted sample annealed at 950°C for 30 s (sweep rate is about 0.07 V/s). Straight lines connect the last datum of each branch. (b) Flatband voltage shift ΔV_{fb} calculated from capacitance-voltage data from (a) and Ref. 13 using Eq. (9) (□). The broken line corresponds to the simulated current-voltage curve A of Fig. 9(a).

about $C_{ox} = 50\,\mathrm{pF}$. This rapid shifting of the C-V curves enables a novel measurement where during the voltage sweep capacitance and current data are simultaneously recorded to trace the charging of the NC's as a function of sweep time and the applied gate voltage V_{gate} [see Fig. 12(a)]. The vertical branches in the I-V characteristic reflect the exponentially decaying charging current with time at constant V_{gate} which is mirrored in the C-V characteristic confirming the interpretation of the I-V characteristics in previous chapter. Continuous charging of the Ge NC's with holes leads to a simultaneously decreasing flat-band voltage, i.e., the C-V characteristic follows the applied gate voltage. In Fig. 12(b) the corresponding flat-band voltage shift ΔV_{fb} is shown as a function of V_{gate} which is calculated from the capacitance data in Fig. 12(a).

$$\Delta V_{fb}(V_{gate}, t) = V_{meas}(C_{meas}, t) - V_0(C_{meas}) \qquad (9)$$

Related to the same capacitance data C_{meas}, the corresponding voltage values from the measured characteristic in Fig. 12(a) (V_{meas}) are referenced to voltage data V_0 from the C-V characteristics for the uncharged state (obtained from the same sample at $\mathrm{d}V_{gate}/\mathrm{d}t = 100\,\mathrm{V/s}$ shown in Ref. 13). ΔV_{fb}, i.e., the total charge stored in the NC's, saturates with increasing FN current [symbols in Fig. 12(b)] which limits the shifting of the C-V characteristic as indicated by the hump in Fig. 12(a). Holes captured in the NC's are compensated with electrons injected from the gate electrode. For the same reason the C-V hysteresis in Fig. 11(b) saturates at $\pm 7.5\,\mathrm{V}$ sweep amplitudes for the Ge, HD implanted sample. However, the trend of the characteristics in Fig. 12(b) is similar comparing the data deduced from the continuous capacitance-current measurements with the results from the simulated current-voltage curves. Thus, the validity of the presented electrical model for the charge transfer through NC containing gate oxides is clearly confirmed. Deviations can be explained by uncertainties defining the exact position of stored and compensated charges within the gate oxide and/or the different sweep rate. For further decreasing V_{gate} a decreasing charge amount is shown in Fig. 12(b) (dashed line) as the electron current is higher than the number of available and refilling holes in the NC's in the simulations for Fig. 9(a). This behavior is not reproduced from the data extracted from Fig. 12(a) since a reliable interpretation of the recorded data is not possible if C_{meas} approaches C_{ox} for $V_{gate} < -14\,\mathrm{V}$.

V. SI NANOCRYSTAL CONTAINING GATE OXIDES

A. Formation of Si NC's in thin gate oxides after Si ion implantation

Ion profile calculations in Fig. 13 reveal a broad distribution of implanted Si in SiO_2 (line). But taking surface sputtering and a redistribution of oxide atoms during implantation into account, a nearly constant total Si content throughout the oxide can be expected (symbols). For Si, HD implantation the incorporation of additional Si in SiO_2 causes a considerable fluence dependent oxide swelling which corresponds to a broadening of the oxygen signal in the RBS spectra in Fig. 14 (see Ref. 40 for details). A 3D kinetic lattice Monte Carlo (KLMC) simulation was used to simulate the redistribution of excess Si and the formation of Si NC's from a SiO_x layer ($x < 2$) during annealing.[21,41] For the simulation the initial configuration was deduced from the calculated TRIDYN Si data, LD (Fig. 13), which leads to a cross-section image as shown in Fig. 15(a). With increasing simulation (or annealing) time Si monomers bundle to precipitates

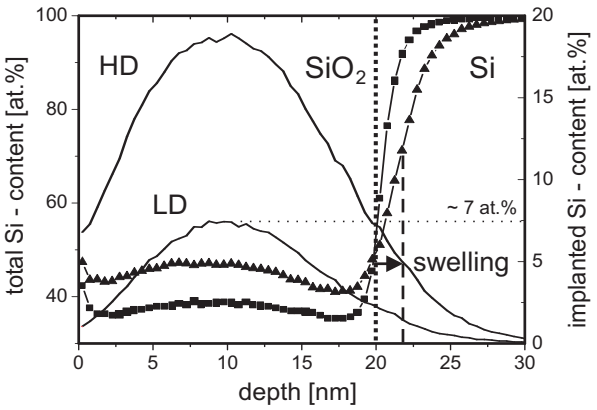

FIG. 13: Total Si content after Si ion implantation into 20 nm SiO_2 [LD (■) and HD (▲)] as obtained from TRIDYN calculations[35] taking sputtering and swelling effects into account (dashed line). The dotted line indicates the pristine position of the Si/SiO_2 interface. The implanted Si profiles (right ordinate) are given by straight lines.

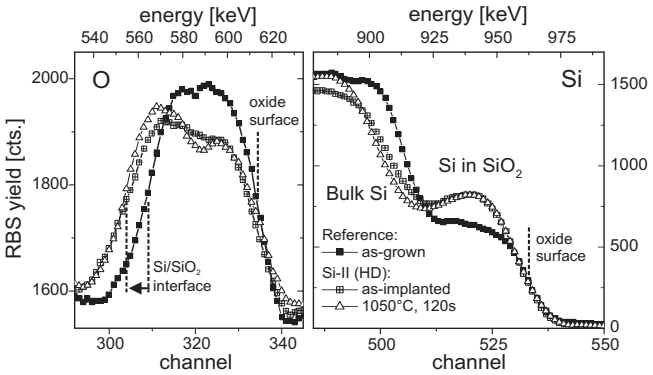

FIG. 14: RBS data related to the oxygen and silicon signals for the high-fluence Si implanted oxide (HD) in the as-implanted state (⊞) and after annealing at 1050°C for 120 s (△) in comparison to the as-grown reference sample (■). The elemental composition of the oxide changes after Si ion implantation by an enhanced Si signal and a reduced O yield with respect to the unimplanted reference.

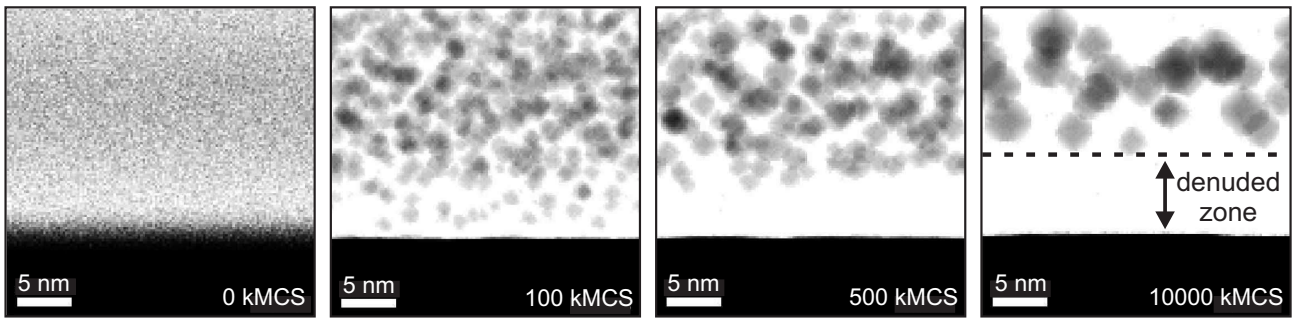

FIG. 15: Cross-section presentation of a KLMC simulation for the Si, LD implanted gate oxide. The initial distribution of Si excess atoms is deduced from TRIDYN calculations in Fig. 13. With proceeding simulation/annealing time [increasing Monte Carlo steps (MCs)] the formation and ripening of Si NC's in the oxide can be traced leading to reconstruction of a flat Si/SiO_2 interface, which is finally separated to the NC's by a denuded zone.

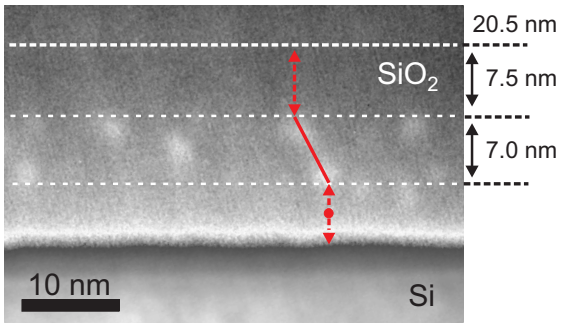

FIG. 16: Cross-section energy-filtered TEM micrograph for the Si, LD implanted sample annealed at 1050°C for 30 s. Some small Si NC's (≤ 2 nm) are visible by bright spots mainly in the oxide center enclosed by two oxide regions denuded of NC's toward the oxide surface and the Si substrate. By conventional high-resolution bright field TEM imaging these tiny Si NC's were not detectable. A red line indicates a localized charge transfer through the oxide across a small portion of NC's.

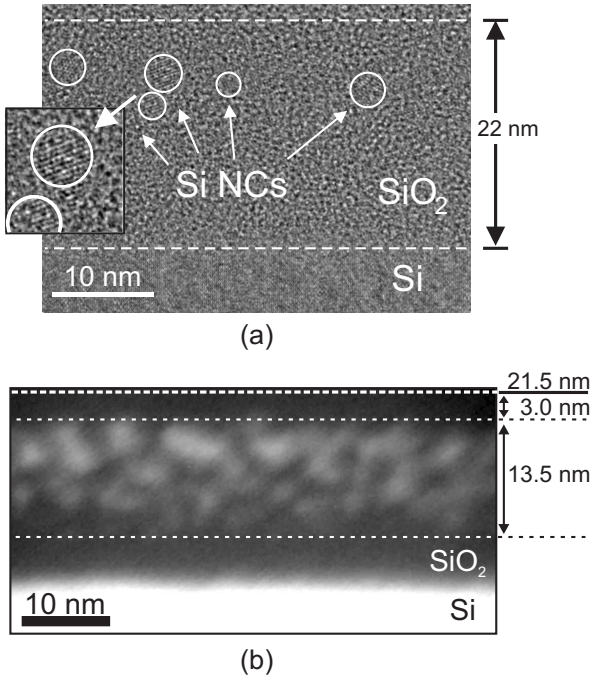

FIG. 17: Cross-section TEM micrographs of a Si, HD implanted sample annealed at 1050°C for 30 s obtained (a) at high resolution bright field conditions and (b) - enabling a much more detailed view on the NC's distribution - by energy-filtered imaging. In (a) at the top region of the oxide layer Si NC's formed with the evidence of Si (111) lattice fringes. About two-thirds of the oxide are filled with Si NC's, visible by bright spots, in a high density, enclosed by two oxide regions denuded of NC's.

mainly in the upper half of the oxide and grow to NC's later on. Despite considerable mixing of the Si/SiO_2 interface during implantation (see Fig. 13), a flat interface between the oxide and the Si substrate reconstructs during annealing. From Gibbs-Thompson's rule, assuming the Si substrate as a crystal of infinite radius, the equilibrium concentration of Si monomers around the embedded Si NC's in oxide is higher than directly above the Si substrate leading to a diffusion of Si monomers from the NC's toward the Si substrate. Some Si NC's located closer to the substrate dissolve whereas those in the upper oxide region ripen. This behavior is confirmed by the redistribution of oxygen during annealing in the RBS spectra of Fig. 14 for Si, HD implantation. The development of a small valley and a little hump in the oxygen profile corresponds to a formation of Si NC's next to the oxide center and a formation of a region denuded by Si NC's close to the Si/SiO_2 interface, respectively.

For the present Si implanted samples Si NC's of 2 - 4 nm size were detected mainly about the oxide center using HR- and EFTEM in Fig. 16 and 17. As predicted by KLMC simulation actually a denuded oxide zone separates the Si NC's from the Si substrate; but, in contradiction, the amount of remaining excess Si forming NC's is much lower than expected. However, in the simulation a

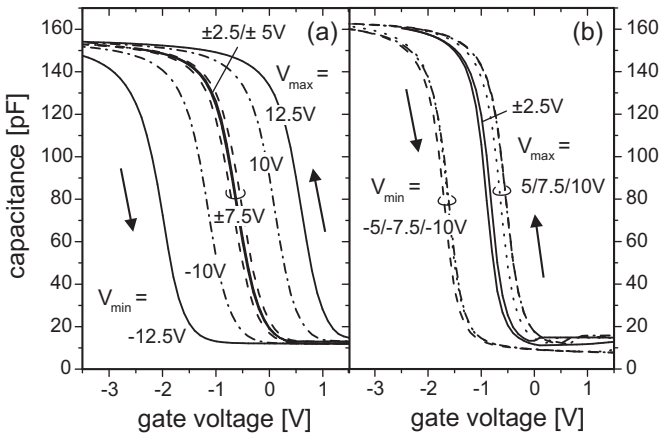

FIG. 18: C-V hysteresis characteristics for the Si, LD (a) and HD (b) implanted gate oxides annealed at 1050 °C for 120 s and 30 s, respectively (the complemental samples show similar charging behavior). Sweep direction is $V_{min} \rightarrow V_{max} \rightarrow V_{min}$ for $\pm 2.5\,\mathrm{V}/\pm 5\,\mathrm{V}/\pm 7.5\,\mathrm{V}/\pm 10\,\mathrm{V}/(\pm 12.5\,\mathrm{V})$. Using quasi-static and conductance C-V methods (not shown) at midgap a Si/SiO_2 interface trap density of $D_{it} \lesssim 1\times10^{11}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ was obtained indicating a sufficient reconstruction of the Si/SiO_2 interface for both fluences.

loss of excess Si from sample handling and annealing after ion implantation was not included.[19,42] When a damaged thin gate oxide is exposed to humid air after implantation, moisture (e.g. O_2 and H_2O) penetrates the porous oxide, which leads - together with residual oxygen from the annealing ambient - to a significant reduction of Si available for NC formation due to oxidation of excess Si. Most sensitive to penetrating oxidants, in the experiment a NC-free region (3 - 7 nm) forms close to the oxide surface (see Figs. 16 and 17), similar to a passivation of bare Si surfaces. This oxide layer can be considered as an efficient top-oxide barrier. Assumedly, the denuded zone between the Si NC's and the Si substrate has not that quality. As shown in Fig. 15(b) incorporated Si precipitates possibly remain in this layer during annealing and enable a considerable charge conduction through this oxide zone like traps. Thus, the respective structural parameters needed for the I-V characteristic calculations are deduced from Fig. 16 and 17 and summarized in Tab.V. Within the denuded zone a trap-like state is considered in d_{nc1} of 1 nm size dividing the denuded zone into the sections d_{tox1} and d_{tox2}.

B. C-V hysteresis of Si NC containing gate oxides

In C-V hysteresis measurements a sweep amplitude higher than 7.5 V (LD) or 2.5 V (HD) has to be applied to show a considerable charging of the Si implanted oxides (see Fig. 18). Positive and negative charges are generated or trapped in the oxide applying negative and positive gate voltages, respectively. Thus, a dominating charge exchange between the Si NC's and the Si substrate can be considered. Whereas the hysteresis increases with increasing gate voltage above a threshold value nearly symmetrically in Fig. 18(a) (LD fluence), the flatband voltage shift saturates for the Si, HD implantation at a comparably low level. This limitation indicates re-emission of trapped electrons toward the gate or compensation of stored holes by electrons injected from the gate. Best observable in the difference of the maximum capacitance values C_{max} comparing Fig. 18(a) and (b), the content of remaining non-oxidized Si merged into Si NC's is much higher for the higher Si fluence. As a consequence the actual oxide dielectric constant changes from $\varepsilon_{ox} = 3.9\,\varepsilon_0$ (virgin oxide) to effectively about $4.35\,\varepsilon_0$ for the Si, HD implanted sample ($\varepsilon_{si} = 11.8\,\varepsilon_0$). For the lower Si fluence, oxide growth (e.g. by oxidation) compensates the effect of remaining excess Si in the oxide ($C_{max} \approx \varepsilon_{ox}/d_{ox}$) as C_{max} is similar to the virgin oxide (not shown).

TABLE V: Structural parameters used in the calculation of the I-V characteristics in Fig. 19 for the Si^+ implanted oxides (LD and HD) and for the un-implanted reference (virgin). Oxide and NC layer sizes are in nm.

fluence	curve	d_{tox1}	d_{nc1}	d_{tox2}	d_{nc2}	d_{top}	d_{ox}
LD	A	2.0	1.0	2.5	7.0	7.5	20.0
HD	B	1.8	1.0	2.0	13.5	3.0	21.3
-	C	-	-	-	-	-	20.7
(LD)	D	-	-	-	-	-	7.5
(HD)	E	-	-	-	-	-	3.0

C. I-V characteristics for the Si implanted oxides

For the Si ion implanted and annealed oxides the currents increase rapidly already above $|\mathrm{V}_{gate}| \approx 2\,\mathrm{V}$ (HD) or $|\mathrm{V}_{gate}| \approx 5\,\mathrm{V}$ (LD) as shown in Fig. 19. Below this voltage the current level is similar to the virgin oxide without significant enhancements which coincidences with the missing C-V hysteresis is this regime (Fig. 18). Apparently, on the contrary to the characteristics for the Ge implanted oxides (Figs. 9/10), the charging does not affect homogenously large area portions. Considerable charge trapping occurs only at high currents (Fig. 19), e.g. at $\pm 12.5\,\mathrm{V}$ (LD) or $\pm 5.0\,\mathrm{V}$ (HD) bias, as confirmed by the C-V hysteresis measurements in Fig. 18. But the obtained V_{fb} shift is 5 - 10 times lower than for the Ge implanted oxides. Changes in the I-V characteristic with increasing annealing time are of minor relevance. At high current densities ($J > 1\times10^{-6}\,\mathrm{A/cm}^2$) the slopes weaken only slightly in the semi-logarithmic plot.

Apparently, for the present Si implanted samples the charging occurs not rather homogenously across a high density of NC's close to the Si substrate, as in the case of Ge containing gate oxides, but across rare defects or traps located in the denuded zone as indicated in Fig. 16. Figure 15(b) shows a considerably high density of such

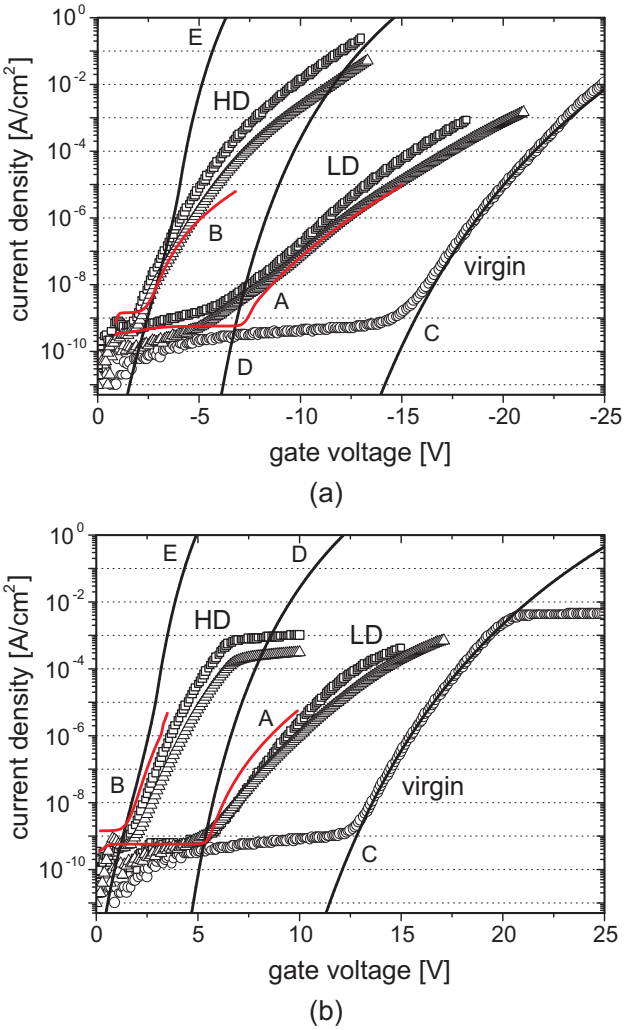

FIG. 19: (Color online) Measured and calculated I-V characteristics for the Si implanted [fluence LD and HD, annealed at 1050 °C for 30 (□) and 120 s (△)] and for the un-implanted oxides (◯) for both gate voltage polarities with respect to Eqs. (1)-(2), solved for 1% capacitor area and Table V. The calculated characteristics for Si NC containing oxides are indicated by red lines (A and B) and for single oxides by black lines (C - E) with V_{fb} = -0.8 V, V_t = 0.1 V and $m_{ox} = 0.5\, m_0$. Measurements and simulations were performed for 0.125 V/s sweeps.

Si precipitates in this region, which disappear bit by bit during further annealing/simulation time. Thus, in a first approximation, the current through the gate oxide for Si implanted oxides J_{si} occurs locally across about 1% of the MOS capacitor area. But, the transient enhanced model as derived in Ref. 13 is only valid for rather homogenously charged oxides. Thus, Eq.(1)-(8) were used to calculate the current only at the involved areas with $R_{nc1} = R_{nc2} = 1$ and $J_{si} = 0.01 \times J_{tot}$ [Eq.(2)]. A band gap energy of 1.4 eV[36] for about 3 nm tiny Si NC's leads to a tunneling barrier of about 3.0 eV for electron ejection from Si NC's.[13] With these assumptions and the

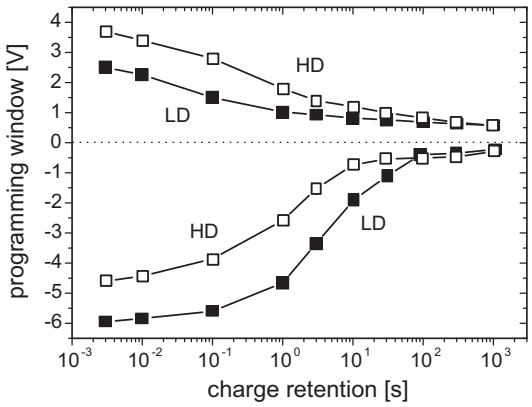

FIG. 20: Retention data for Ge implanted oxides for both fluences, LD and HD, after programming pulses of ± 8V applied for 100 ms. The programming window reflects the difference of the actual $V_{fb}(t)$ to the initial (uncharged) state with the positive and negative voltage branch indicating storage of electrons and holes, respectively.

structural data from Tab. V the calculated I-V characteristics show significant agreements, qualitatively and quantitatively, with the measurements. Again, the onset of the high current regions in Fig. 19 coincidences with the characteristics related to MOS capacitors containing only the top-oxide layer d_{top}.

VI. CHARGE STORAGE IN GE AND SI NC CONTAINING OXIDES

For the embedded Ge NC's initially large programming windows are obtained (about 8 V) in Fig. 20, which decay within the first seconds to a more stable state holding about 1 V for more than minutes. Thus, two different charge loss mechanisms can be considered: The first loss (short term storage) is considerably attributed to a spontaneous re-emission of electrons (or holes) from the NC's band edges toward the Si substrate. Also injection of holes (or electrons) from the substrate side has to be taken into account leading to a charge compensation in the NC's. A different back-tunneling barrier height for electrons and holes ($\phi_{b,e} < \phi_{b,h}$) (or, alternatively, a shorter generation time of holes than of electrons from a p-Si substrate) causes slightly different time scales of charge decay. Capture of electrons at self-interstitial defect sites located at or in the Ge NC's[43] might be responsible for the long term storage as well as the different relative band gap position of the Ge NC's in comparison to the Si substrate (hole storage).[13]

On the contrary to the Ge implanted samples, stored electrons and holes hold in the present Si NC containing structures at least for hours as shown in Fig. 21. According to the presented model of charge conduction, the rare small traps embedded in the denuded zone between the NC's and the Si substrate limit efficiently the loss toward the substrate electrode. From extrapolations quasi

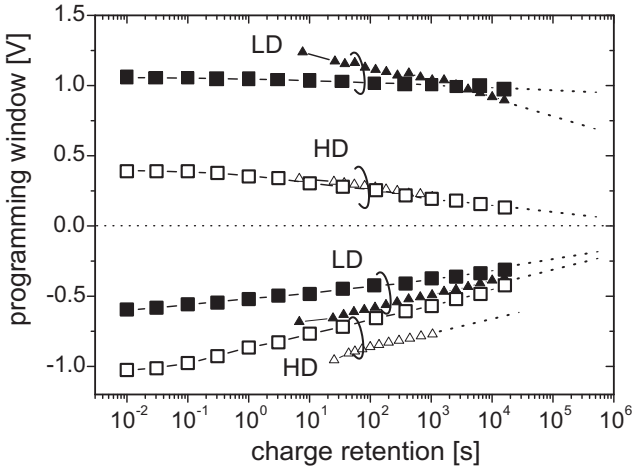

FIG. 21: Charge retention characteristics for the Si implanted samples (LD and HD with filled and open symbols, respectively), representing the behavior after 10 (squares) and after 10^5 (triangles) write/erase cycles after applied voltage pulses of $\pm 12.5\,\mathrm{V}$ (LD) and $\pm 5\,\mathrm{V}$ (HD) for 100 ms.

non-volatility up to real non-volatility can be predicted depending on the implanted Si ion fluence. For the Si, LD implanted sample the programmed and the erased states should be distinguishable from each other up to days and months ($> 10^6\,\mathrm{s}$), even if this device has been previously treated with 10^5 write/erase cycles. Especially for the Si, LD sample, device cycling widens slightly the programming windows with the consequence of an increased charge decay with retention time. During cycling at high electrical fields and high current stress needed in the write/erase operations, oxide traps are generated, which mediate a charge transfer toward the NC's, but enable also a faster escape of charges from the NC's toward the substrate or gate electrode.

VII. SUMMARY

An electrical model has been developed to describe current-voltage characteristics for thin NC containing gate oxides. Ion beam synthesis of Ge and Si NC's in SiO_2 leads to different spatial distributions, varying from narrow NC layers close to the Si substrate to broad layers spanning around the oxide center. From these structural data current-voltage characteristics were calculated, which show significant qualitative and quantitative agreements with measurements, considering significant charging of the NC's. Oxide layers denuded of NC's, which form self-organizing during annealing, work efficiently as charge tunneling barriers. Thus, ion implantation induced oxide traps are not responsible for the charge transfer through the oxide. However, in some cases a trap-assisted conduction is proposed between the Si substrate and the NC layers or between NC's. Monte Carlo Simulations reveal that these traps might evolve from dissolving Si (or Ge) precipitates in the oxide close to the Si/SiO_2 interface, for instance. Ion profile calculations related to NC synthesis in thin gate oxides are not suitable to predict the final NC distribution since also redistribution and oxidation effects have to be taken into account. The obtained charge retention in the NC containing gate oxides spans from seconds or minutes (Ge NC's) to the perspectives of quasi non-volatility (Si NC's) with a charge retention of months or more depending on the number of performed write/erase cycles before measurement.

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9 Dissociation of implanted and as-grown thin oxide layers during annealing at low partial pressure of oxygen

Dissociation of Si^+ ion implanted and as-grown thin SiO_2 layers during annealing in ultra-pure neutral ambient by emanation of SiO

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We have observed a very inhomogeneous dissociation of stoichiometric and non-stoichiometric thin SiO_2 layers (thermally grown on Si substrates) during high temperature annealing at a low partial pressure of oxygen. During this process some silicon of the (100)Si substrate and, in case of Si ion implantation, additionally excess Si is consumed. The SiO_2 dissociation has been studied by electron microscopy and Rutherford backscattering spectrometry. Large holes ($>1\,\mu$m) in non-implanted oxide layers have been observed which evolve probably from defects located at the Si/SiO_2 interface. For Si implanted SiO_2 additionally the formation of voids within the oxide during annealing has been observed preferably at the position of the implanted Si excess. Oxygen vacancies are possibly emitted from Si/SiO_2 interfaces into the oxide and migrate through SiO_2 with long-range distortions of the oxide network. In that way the oxide hole and void formation can be explained by oxygen-vacancy formation, migration and silicon-monoxide (SiO) emanation. As a driving force for growth of the large oxide holes we identified oxygen diffusion from the Si/SiO_2 interface to the bare Si surface. This surface is a sink of oxygen diffusion due to the emanation of volatile SiO, whereas the Si/SiO_2 interface serves as an oxygen source. The predicted mechanism is consistent with the geometry of the holes in the SiO_2 layer.

I. INTRODUCTION

It is well known that heat treatment under ultra-high vacuum conditions results in a very inhomogeneous dissociation of thin SiO_2 films on Si.[1] Small, circular holes were found in the oxide with areas of bare Si substrate completely depleted from SiO_2. The process of dissociation was assigned to diffusion and evaporation of SiO starting at the Si/SiO_2 interface.[1] It was concluded that these molecules diffuse through SiO_2 towards the surface where SiO finally desorbs.[2,3] A model of the generation of volatile SiO at the Si/SiO_2 interface was proposed by Hickmott[4] by the reaction

$$\mathrm{Si}_{(s)} + \mathrm{SiO_2}_{\,(s)} \rightarrow 2\,\mathrm{SiO}_{(g)}\uparrow . \qquad (1)$$

Although it was argued that this molecule is too large to diffuse through the SiO_2 network,[5] experiments show that under special annealing conditions thermally grown SiO_2 acts as a source of oxygen for the underlying Si bulk.[5] A reduction of SiO_2 was proposed by Balk *et al.*[6] where a redox reaction leads to the formation of neutral oxygen vacancies (V_o) in SiO_2. The released oxygen atoms diffuse to the Si/SiO_2 interface and are consumed by the oxidation of Si.

$$\mathrm{O_3{\equiv}Si\text{-}O\text{-}Si{\equiv}O_3} \rightarrow \ \mathrm{O_3{\equiv}Si\text{-}Si{\equiv}O_3} + \mathrm{O}\uparrow \qquad (2)$$

The neutral oxygen vacancy is known to be an amphoteric trap,[7] mainly associated with hole traps from the so called oxygen-deficiency centers which are generated during high temperature annealing of oxides due to a removal of oxygen.[8,9]

With respect to the understanding of Si/SiO_2 interface microchemistry and the formation of Si (or Ge) nanocrystals (NCs) within thin SiO_2 films for microelectronic or optical devices, the self-diffusivity of Si and O in SiO_2 has received much interest in the recent two decades. Several direct[10] and indirect methods[11–14] have been applied to determine diffusion parameters (D_0, E_A), e.g. the implantation of ^{30}Si isotopes in $^{28}SiO_2$ layers.[12,15] But the data for the Si self-diffusivity differ by several orders of magnitude depending on the processing parameters. The activation energy for the diffusion of Si as found by Tsoukalas *et al.*[12] (4.7 eV) is also remarkably close to those for the diffusion of network oxygen.[16] A higher diffusivity derived from indirect experiments was attributed to a diffusion of SiO molecules instead of self-diffusion of Si atoms.[17,18] In addition, it was reported that mobile SiO might have a catalytic effect on the thermomigration of impurities[17] and on the enhancement of the self-diffusion of Si in SiO_2.[19]

In the present work, after annealing in ultra-pure Ar atmosphere an inhomogeneous dissociation of thermally grown SiO_2 is described and compared to the behavior of Si implanted oxides. Several diffusing species have been considered with different mechanisms of diffusion in SiO_2. But a general description has to be consistent with both, oxide hole formation and Si self-diffusion, whereas contradictions give new insights. In particular, the artificial Si enrichment, which intensifies internal reactions, reveals additional information concerning the mechanisms of diffusion in and finally dissociation of SiO_2. The investigations are of practical relevance for the annealing of Si implanted gate oxides designed for non-volatile memory devices.

II. EXPERIMENT

$^{28}Si^+$ ions were implanted at 6 keV with fluences of $7{\times}10^{15}\,\mathrm{cm^{-2}}$ (LD) and $2{\times}10^{16}\,\mathrm{cm^{-2}}$ (HD) at room temperature in 20 nm thick SiO_2 thermally grown on <100>

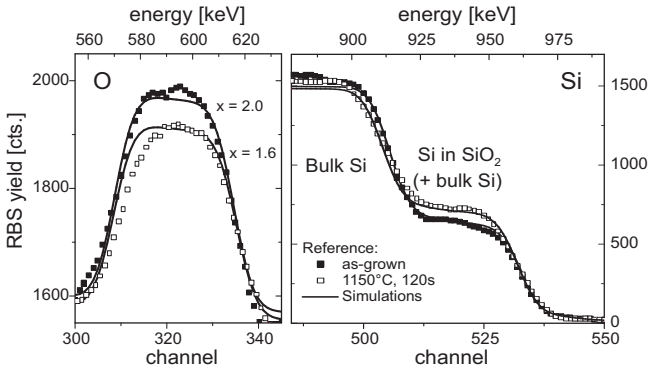

FIG. 1: Oxygen and Si related parts of the RBS spectra for the as-grown (■) and the tempered (□) (1150°C for 120 s) reference samples in comparison to a simulation for 20 nm thick SiO_x layers with x = 2 and x = 1.6 (lines), respectively. Within all RBS graphs the experimental data are smoothed by a Savitzky-Golay algorithm to show differences in the results more clearly.

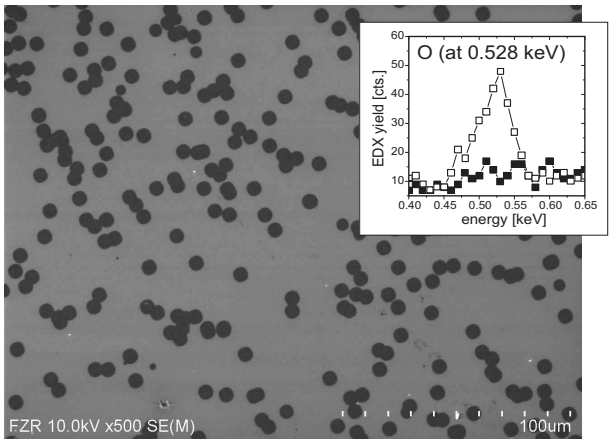

FIG. 2: SEM image of the unimplanted reference tempered at 1150°C for 120 s in ultra-pure Ar ambient. The gray area indicates SiO_2 and the dark spots bare silicon substrate (oxide holes) as confirmed by EDX (10 keV, $2\times2\,\mu m^2$) shown in the inset (oxide: □; hole : ■).

p-Si substrate (10 Ω cm). Not-implanted samples with identical SiO_2 films were used as references. After standard cleaning in H_2O_2/H_2SO_4, rapid thermal annealing (RTA) was carried out at 1050°C and 1150°C for 30 s and 120 s in Ar, respectively. The Ar gas quality was improved from 5.0 to 9.0 (1 ppb) with respect to oxidants (e.g. O_2, H_2O) by means of a gas purifier. Similar experiments were performed for 100 nm thick SiO_2 with an implantation of $4\times10^{16}\,cm^{-2}$ Si ions at 35 keV. The Si and O profiles were characterized by Rutherford backscattering spectrometry (RBS) using 1.7 MeV He^+ ions; the incident angle was set to 70° to improve the depth resolution (scattering angle is 170°). Transmission electron microscopy (TEM) on a Philips CM300 operating at 300 kV as well as scanning electron microscopy (SEM) on a Hitachi S-4800 at 10 kV were carried out

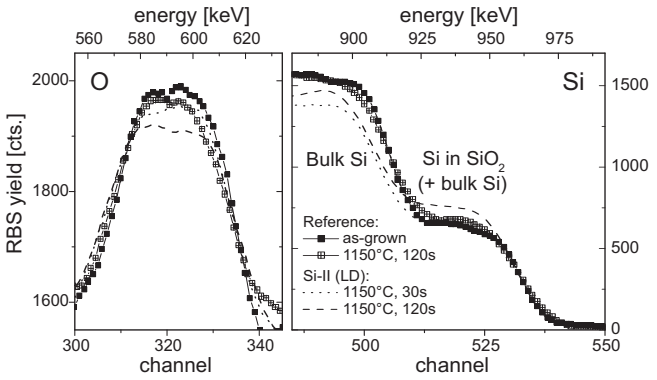

FIG. 3: RBS data for a low-fluence Si^+ implanted oxide (LD) compared with the reference sample both annealed at 1150°C. A partially lower yield from the Si bulk at the right graph is attributed to substrate channelling.

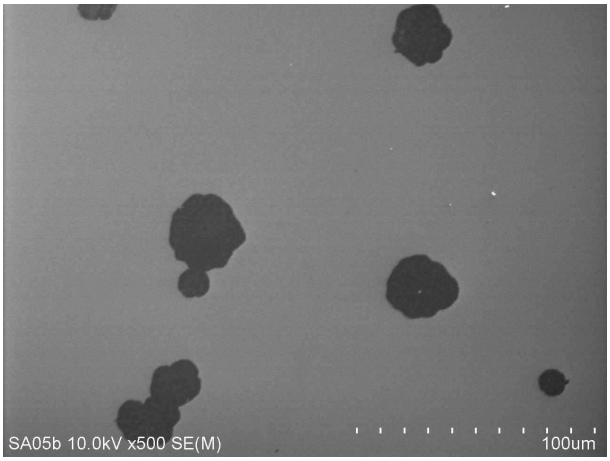

FIG. 4: SEM image of a Si^+ implanted (LD) sample after subsequent annealing (1150°C for 30 s). Oxide holes of non-uniform size (∼15..40 μm) and shape are obtained.

for structural investigations including energy-dispersive X-ray (EDX) analysis for local element mapping.

III. RESULTS AND DISCUSSION

As shown in Fig. 1 already the unimplanted thermally grown oxide reveals changes in the RBS spectrum after a heat treatment at 1150°C. These can be interpreted either as a change of the oxide stoichiometry (from SiO_2 to $SiO_{1.6}$) or as lateral oxide inhomogeneities. The latter explanation is clearly confirmed by the respective SEM image shown in Fig. 2. Nearly circular areas of bare Si with impressively regular size (∼6 μm) and shape are observed. These oxide holes cover about 20% of the total surface area explaining the increase and reduction of the Si and O signals in the RBS spectrum of Fig. 1, respectively. The deviation in Fig. 1 between simulation and measurement at the low energy side for the annealed ref-

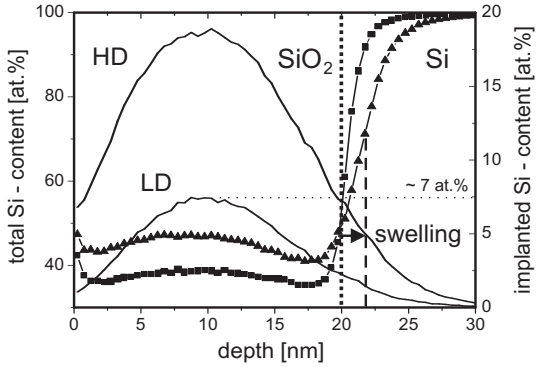

FIG. 5: Total Si content after Si ion implantation into 20 nm SiO_2 [LD (▲) and HD (■)] as obtained from TRIDYN calculations[21] taking sputtering and swelling effects into account. The dotted line indicates the pristine position of the Si/SiO_2 interface. The implanted Si profiles (right ordinate) are plotted by straight lines.

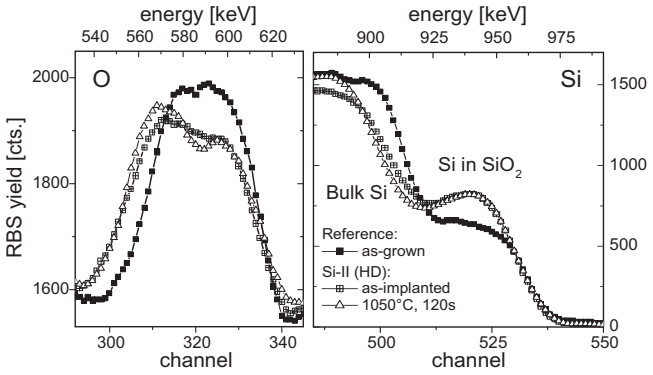

FIG. 6: RBS data related to the oxygen and silicon signals for the high-fluence Si implanted oxide (HD) in the as-implanted state (⊞) and after annealing at 1050°C for 120 s (△) in comparison to the as-grown reference sample (■).

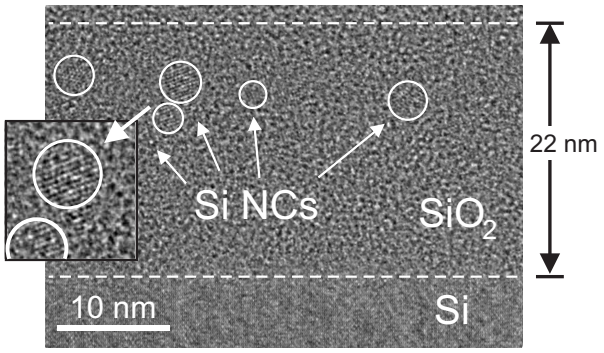

FIG. 7: High resolution cross-section TEM image of a HD implanted sample annealed at 1050°C for 30 s. At the upper region of the oxide layer Si NCs formed which is proved by the evidence of Si (111) lattice fringes.

erence (best observable in the oxygen related data) might correspond to a global non-uniform thickness reduction of the remaining SiO_2 layer and/or in an increased Si/SiO_2 interface roughness which cannot be decided from the RBS data. The detected local dissociation of SiO_2 is similar to the results published by Tromp *et al.*[1] and Liehr *et al.*[20] They argued that the SiO_2 decomposes by the formation of volatile SiO [acc. Eq. (1)] at defects in the oxide or at the Si/SiO_2 interface which are not specified in detail. The statistically distributed but equal-sized and -shaped oxide holes obtained for the tempered reference (Fig. 2) indicate that heteronucleation at one single type of defect is responsible for the inhomogeneous SiO_2 dissociation.

The situation is not generally changed for low-fluence (LD) Si^+ implantation (Fig. 3). The oxygen areal density is reduced after annealing (1150°C for 120 s) in a similar way as observed for the reference before. But now, the oxide holes, indicating the local dissociation of SiO_2, are irregular in shape and size (Fig. 4). The similar oxygen content confirms that with respect to the annealed reference the mean oxide hole coverage is equivalent despite the significant differences in size and density of the holes. The lower hole density and the larger hole size indicate, that for the implanted oxides an accumulation or a local concentration of such defects, which are responsible for the SiO_2 dissociation, occurs, induced by ion implantation and subsequent annealing.

The incorporation of additional Si into SiO_2 by ion implantation causes a fluence dependent oxide swelling (see Fig. 5) which corresponds to a broadening in the oxygen signal of the RBS spectra for the LD (Fig. 3) and HD (Fig. 6) implanted oxides, respectively. In addition, RBS clearly reveals the change in the elemental composition of the oxide after Si ion implantation by an enhanced Si signal and a reduced O yield with respect to the unimplanted reference.

Phase separation of Si from SiO_2 occurs by precipitation and growth of Si NCs during annealing at 1050°C. These processes are induced either by (i) self-diffusion of oxygen or (ii) of the implanted excess Si or (iii) the diffusion of mobile SiO molecules, depending on the favored model of diffusion as mentioned before, or (iv) by a process involving diffusing oxygen vacancies which we will discuss later in detail. As indicated by the small valley in the oxygen profile (Fig. 6) the Si NCs are mainly located within the upper half of the oxide layer which is confirmed by cross section TEM imaging (see Fig. 7). No SiO_2 dissociation has been observed for an annealing at 1050°C.

A strong dissociation of the HD implanted SiO_2 is obtained after annealing at 1150°C. As shown in Fig. 8 the RBS spectra reveal a remarkabe decrease of both, the Si and the O areal density. The oxygen content is reduced by ∼30% and ∼65% after annealing at 1150°C for 30 s and 120 s, respectively. In agreement with the effects described before, again a spatial dissociation of the oxide is expected and confirmed by SEM (Fig. 9) showing a very high concentration of tiny ($\ll 1\,\mu$m) oxide holes.

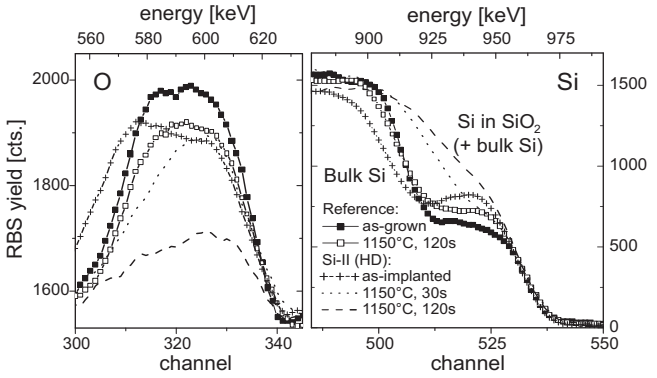

FIG. 8: RBS spectra of the high-fluence Si implanted oxide (HD) as-implanted (+), annealed at 1150°C for 30 s (dotted line) or 120 s (dashed line), respectively, in comparison to the as-grown reference sample (■) tempered at 1150°C (□) for 120 s.

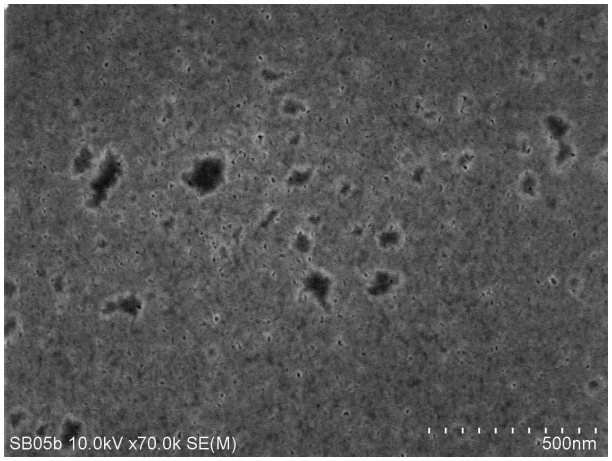

FIG. 9: SEM image of the high-fluence Si implanted sample (HD) after annealing at 1150°C for 30 s. The oxide holes (black regions and tiny spots) are of different sizes (30..200 nm; spots: < 10 nm) with irregular shape but in a very high density.

Despite the very different size distribution and density of holes, the mean oxide/hole area ratio is nearly equivalent to the annealed reference. But contrariwise to the samples described before the dissociation of SiO_2 is not anymore only a lateral effect. As shown in the TEM image of Fig. 10(a) in the region where previously the Si NCs within the oxide were detected (Fig. 7), nanopores (NPs) (or nanovoids) have formed after 1150°C annealing . The residual top and bottom oxides are connected by a porous oxide network or only single oxide columns. The residual oxide thickness is ≤ 20 nm which explains the narrowing of the oxygen signal in the RBS spectra (Fig. 8). Besides the NP formation, the residual oxide is more or less stable in shape and height. With respect to the annealed reference the oxygen content of the implanted sample (HD after annealing at 1150°C for 30 s) is lowered by $\sim 1.8\times10^{16}$ O/cm^2. As the oxide to hole

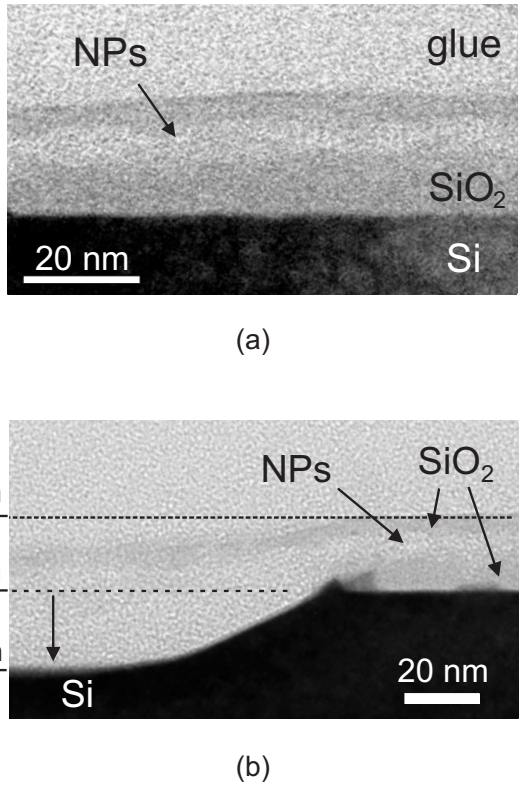

FIG. 10: TEM images of the high-fluence Si implanted sample (HD) after subsequent annealing at 1150°C for 120 s in purified Ar. (a) Voids or nanopores (NPs) have formed in the upper half of the oxide dividing the layer into two parts. In (b) almost all SiO_2 has disappeared (left side) together with a part of the Si substrate where residual oxide is still overhanging.

areal ratio remains unchanged, this additional loss must be related to the internal dissociation of the oxide. The oxygen loss corresponds to the Si implantation fluence of 2×10^{16} cm^{-2} (HD) which is a strong hint for the formation of volatile SiO molecules preferably within the region of the implanted Si excess. The required oxygen amount is probably taken from the SiO_2 network environing the Si NCs e.g. by a redox reaction similar to Eq. (2) leaving oxygen vacancies or deficiency centers behind. The reaction stops when the implanted Si amount has been consumed.

The formation of the oxide holes is certainly no oxide surface effect. Similar experiments performed with 100 nm SiO_2 reveal no observable oxide dissociation even after a heat treatment at 1150°C for 120 s performed in ultra-pure Ar ambient. Thus, the process has to be interpreted as diffusion controlled and forced by Si/SiO_2 interfaces. In fact, the implantation at the higher fluence (HD) causes both, (i) a region of excess Si within the oxide, and (ii) additionally a Si excess within the near interface oxide due to ion-induced interface mixing (see the weaker slope at the Si/SiO_2 interface in Fig. 5). Both regions, there and around the Si precipitates within

the oxide, reveal a considerable concentration of oxygen vacancies leading to the high density of oxide holes in Fig. 9.

In Refs. 1–3 it was argued that SiO molecules are generated at the Si/SiO_2 interface in SiO_2 leading finally to the oxide dissociation. The idea of a single SiO molecule squeezing through SiO_2 can conceivably be unravelled by the idea of diffusion of oxygen vacancies (V_o)[22] taking an interaction of SiO with the surrounding covalent network into account. Diffusion mechanisms in SiO_2 are supposed to be dominated by jumps of dangling bonds rather than by migration of single Si interstitials through SiO_2.[23] *Ab initio* calculations reveal a rather small energy of V_o formation ($\approx 0.85\,\mathrm{eV}$)[24,25] at Si/SiO_2 interfaces and V_o migration ($\approx 1.8\,\mathrm{eV}$)[26] in SiO_2. This is consistent to a high concentration of V_o close to the Si/SiO_2 interfaces especially during high temperature annealing at low partial pressure of oxygen. Migrating oxygen vacancies cause long-range network distortions in the oxide network[27] leading actually to a Si self-diffusion in SiO_2. This explains the considerable dependence of the Si self-diffusivity from the oxide thickness[15] as the concentration of V_o and thus the driving force for Si redistribution increases with decreasing distance to the Si/SiO_2 interface.

Discussing the process of SiO_2 dissociation by vacancy diffusion, the reactions at the Si/SiO_2 interfaces especially around the NCs and at the SiO_2 surface may be expressed as

$$\text{at } Si/SiO_2 \text{ interfaces:} \quad Si + SiO_2 \rightarrow 2\,SiO_2 + 2\,V_o \quad (3)$$

$$\text{at the } SiO_2 \text{ surface:} \quad 2\,V_o + 2\,SiO_2 \rightarrow 2\,SiO_{(g)}\uparrow . \quad (4)$$

Hence, the excess Si in the oxide (due to implantation or interface mixing) accumulates at the Si NCs and is later on oxidized by the formation and emission of V_o. This is consistent with Gibbs-Thompson's relation that small Si NCs dissolve due to the high equilibrium V_o concentration at their curved interface resulting in a growth of bigger ones (like the Si substrate). These vacancies diffuse also towards the region of lower V_o concentration i.e. to the SiO_2 surface, where they may be emanated in form of gaseous SiO under consumption of surface oxide. Obviously the formation energy of such a SiO release is rather high, because no fast homogeneous dissociation of SiO_2 has been observed. But local defects at the Si/SiO_2 interface facilitate SiO formation and emanation, which can finally cause the formation of large oxide holes.

In Fig. 10(a) a formation of large voids within the oxide is observed. There, during high temperature annealing at low oxygen partial pressure, besides V_o also volatile SiO forms at the Si NCs until all excess Si is consumed. Diffusing V_o between the NCs and the oxide surface may open pathways for direct SiO emanation. Thus, it is likely to assume that SiO diffuses through the SiO_2 network under assistance of V_o which can be expressed in combination of Eqns. (1), (3) and (4) by

$$Si + SiO_2 \rightarrow SiO_{(g)}\uparrow + SiO_2 + V_o\ . \quad (5)$$

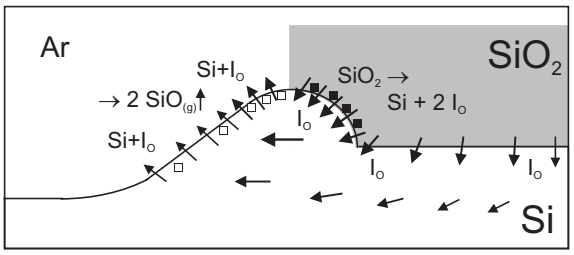

FIG. 11: Sketch of the process of oxide hole growth at the hole rim where a Si hump builds with respect to Fig. 10(b), Ref. 1 and Eqns. (6) and (7).

This is similar to Si interstitial migration in SiO_2 but includes the SiO emanation from the oxide surface. A Si NC oxidation by emission of V_o into SiO_2 as indicated in Eq. (3) has not been observed. NCs would remain after annealing due to size-limiting oxidation.[28] Once a oxide hole has formed as in Fig. 10(b), SiO directly emanates at the hole rim from the NC region into the annealing atmosphere due to its considerable vapor pressure of 10^{-1} mbar at 1150°C.[29,30] A redox reaction acc. Eq. (2) with release of oxygen alone can be fairly excluded. The Si consumption at the Si substrate and within SiO_2 obtained at the outstanding TEM results (Fig. 10) reveals that nearly no oxygen is lost without an oxidizing reaction of Si to SiO there.

For comparison, Si implantation at a lower fluence (LD) has a negligible influence on the internal dissociation of SiO_2. This is most probably due to the oxidation of the implanted Si amount. After ion implantation in SiO_2 at doses $\gtrsim 1\times10^{15}\,\mathrm{cm}^{-2}$ a complete destruction of the SiO_2 network occurs allowing atmospheric moisture to penetrate the oxide when the sample is exposed to normal air.[31] The corresponding additional oxygen content is almost of the same order of the LD implantation fluence. Thus, in this case after annealing the introduced Si can be assumed to be oxidized and adapted to the recovered SiO_2 network leading to a slightly increased oxide thickness without any internal Si/SiO_2 interfaces as needed for a SiO and V_o reaction according to Eqns. (1) and (5), respectively. The SiO_2 dissociation seems not to be affected by the ion induced oxide damage.

Generally, during annealing at 1150°C in ultra-pure Ar ambient a significant part of SiO_2 disappears (see SEM images in Fig. 2, 4 and 9) leaving regions of bare silicon behind. As shown in Fig. 10(b) this process also consumes Si from the substrate; a similar effect was found for the reference sample (not shown). The consumption of bulk Si is a clear indication for a reaction where according to Eq. (1) volatile SiO is formed. At the periphery of the oxide holes humps of Si above the Si/SiO_2 interface plane are observed [Fig. 10(b)]. Such a Si accumulation was also found by Tromp *et al.*[1] but in a much more pronounced manner. The fact that the Si substrate thickness increases slightly at the periphery of the hole towards the Si/SiO_2 interface level indicates that during lateral hole

growth volatile SiO is not formed directly at the Si/SiO_2 interface below the oxide but a few nanometers apart from that. At the oxide hole sidewall and below the remaining oxide oxygen interstitials (I_o) are continuously emitted from SiO_2 into neighbored Si in correspondence to Ref. 5 as shown in Fig. 11. These oxygen interstitials diffuse towards the Si surfaces and form there volatile SiO under the consumption of surface Si.

$$\text{Si/SiO}_2 \text{ interface:} \quad \text{Si} + \text{SiO}_2 \rightarrow 2\,\text{Si} + 2\,\text{I}_o \qquad (6)$$

$$\text{Si surface:} \quad 2\,\text{I}_o + 2\,\text{Si} \rightarrow 2\,\text{SiO}_{(g)}\uparrow \qquad (7)$$

Once, an oxide hole has formed and bare Si is existing the reaction of I_o (diffusion through Si) is dominant against the reaction of V_o (diffusion through SiO_2).

IV. SUMMARY

An inhomogeneous dissociation of as-grown and implanted thin thermally grown SiO_2 films was observed during annealing at 1150°C in a rather oxygen free Ar ambient at normal pressure. During this process not only SiO_2, but also a part of the underlying Si substrate is consumed. The implanted Si excess disappeared under consumption of oxygen from the surrounding SiO_2 by a localized process leaving voids in the oxide behind. Both effects can be explained by the evaporation of SiO. At Si/SiO_2 interfaces and at Si surfaces volatile SiO is generated by oxidation of Si, however, but similar to Eqns. (1), (5) and (7), respectively. Under suitable atmospheric conditions, i.e. low oxygen partial pressure, SiO molecules diffuse mediated by oxygen vacancies through the disturbed or as-grown SiO_2 and evaporate at the oxide surface into the annealing ambient due to its high vapor pressure. These processes are clearly enhanced by ion implantation of excess Si (≥ 10 at.% in the oxide) where oxygen vacancies are generated in a high concentration both at the Si/SiO_2 interface due to ion beam mixing during implantation and around Si precipitates or nanocrystals within the SiO_2. The oxide damage due to ion implantation can be excluded as a reason for SiO_2 dissociation. The growth of an existing oxide hole is clearly not forced by oxygen vacancy formation. Oxygen interstitials are emitted from the oxide at the Si/SiO_2 interfaces into adjacent Si regions. Nearby at bare Si surfaces volatile SiO is formed under consumption of bulk Si and oxygen interstitials.

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10 Summary

Aiming at nanodot memory device applications tiny Ge and Si nanocrystals (NC's) of 1 - 3 nm size are synthesized in thermally grown 20 nm thin gate oxide by low energy ion implantation and subsequent annealing. Depending on the ion element (Ge or Si), energy and fluence the NC's embedded in SiO_2 are formed close to the oxide center or in a δ-like layer close to the Si/SiO_2 interface. As high fluences are needed to yield a supersaturation of impurities inside the oxide necessary for NC formation, dynamic changes in the oxide composition with respect to the initial SiO_2 stoichiometry have to be taken into account during the low energy ion implantation process. As a consequence oxide swelling and a sputtering-related oxide surface recession have to be considered for a reliable ion profile calculation. Here, the ion profiles are adjusted with their maximum close to the oxide center to achieve a limited impact on the Si/SiO_2 interface and Si substrate quality.

In case of such shallow ion implantations in thin oxides the ambience during wafer handling, cleaning and annealing plays a much pronounced role. Moisture components (H_2O vapor, H^+, OH^-) penetrate into the damaged oxide if the wafer is exposed to normal air conditions leading to an enrichment of hydrogen and oxygen in the near-surface oxide. The ion beam synthesis requires an annealing step after the ion implantation to recover the damaged oxide (and Si substrate) and to simulate the NC's growth. At the same time the excess oxygen or hydrogen is available to react, e.g. with Ge to GeO_2 or to mobile (volatile) compounds such as GeH_4 or GeO. For ion beam synthesis of Si or Ge NC's the annealing influences the elemental depth profiles and the corresponding NC distribution in very different way. In case of Ge^+ implantation a considerable Ge redistribution in the oxide towards the Si substrate is observed accompanied by an elemental loss. Here, Ge gains a diffusivity in the oxide which is orders of magnitude higher than that of interstitial Ge. The presented experiments show that both effects, the Ge redistribution and loss, are related to the formation of highly mobile GeO. The loss refers to GeO which meets the SiO_2 surface and emanates into the annealing ambience. A GeO molecule in SiO_2 can be considered to be equivalent to a Ge oxygen-deficient center. Then, the diffusion mechanism is determined by the correlated Ge and oxygen vacancy movement through the oxide, i.e., the enhanced Ge mobility in SiO_2 is here explained as an oxygen vacancy assisted process. In case of Si^+ implantation the Si NC's form mainly in the oxide center without a significant redistribution, whereas the Si excess close to the oxide surface is oxidized to SiO_2. Reducing the impact of oxidants from the annealing ambience, the thermal treatment is performed by rapid thermal annealing in neutral Ar gas at ultra-low partial pressure of oxygen. As a consequence at temperatures of $T > 1100°C$, which are much higher than those needed for Si or Ge NC's synthesis (950 - 1050°C), a dissociation of the Si^+ implanted and also as-grown thin SiO_2 layers is observed and explained by emanation of SiO.

Here, the Ge redistribution effect is advantageously used for the formation of a self-organized δ-like layer of Ge NC's in vicinity to the Si/SiO_2 interface which is a desired configuration to achieve nanodot memory devices with low programming voltage and/or times. The vicinal NC formation derives from a parasitic mixing of the Si/SiO_2 interface if the Ge^+ implantation cascade meets the Si substrate. Small Si precipitates remain in the oxide during the thermally activated interface reconstruction. Mobile Ge (GeO) provided from the oxide depth condenses there leading finally to a considerable growth of Ge NC's. The initial Si precipitates get oxidized by oxygen supplied from the trapped GeO molecules. The Ge NC's are produced at a size of about 2 nm in a very high density of about $3\times10^{12}\,cm^{-2}$. Considering direct tunneling as the dominant charge transfer mechanism from the Si substrate to the Ge NC layer, an electrical model is developed based on a floating-gate-like approach to describe the transient programming characteristics of NC containing thin oxides. Quantum confinement and Coulomb blockade effects of small Ge NC's (1 - 6 nm) are discussed and found to be negligible for the present structure. A close agreement between the calculated write characteristics and experimental data obtained on metal-oxide-semiconductor capacitor devices clearly confirms the validity of the model. As shown, the programming behavior of nanodot memories is mainly determined by the distance of the NC's to the Si substrate. Using this model, for the first time the distribution of the tunneling oxide thickness d_{tox} is determined from simple programming characteristics in high precision as confirmed by high-angle annular dark-field scanning transmission electron microscopy imaging. The evolution of d_{tox} during heat treatment is discussed in terms of Ostwald ripening whereas d_{tox} increases with annealing time. In order to study the leackage current through NC containing gate oxides, current-voltage characteristics are electrically modeled and calculated for gate oxides which contain Si and Ge NC's in different distributions, sizes and densities. Structural data needed for the electrical model are deduced from transmission electron micrographs. The calculated current transfer characteristics show convincing agreements with measurement results. Simultaneous current-capacitance measurements confirm that the internal electrical fields in the oxide are forced by the charged NC's. The leakage currents through the present NC containing ion implanted and annealed thin gate oxides are strongly related to the NC's location and are not driven by defects generated by ion implantation. Especially the Ge NC containing oxides enable short programming times at low voltages but only a short data retention. Thus, the prepared Si or Ge NC containing memory devices show more DRAM-like or quasi-nonvolatile than real nonvolatile behavior.

The main findings can be summarized as follows:

- Tiny Ge and Si nanocrystals were fabricated in thin gate oxides by ion beam synthesis aiming at nanodot memory devices.
- For a reliable calculation of high fluence low energy ion implantation profiles dynamic changes of the oxide composition have to be taken into account, e.g. the swelling of the oxide and the surface recession due to sputtering.
- Moisture penetrates the damaged oxide due to sample exposure to normal air, cleaning and annealing ambiences leading to an enrichment of the oxygen and hydrogen

content in the near-surface oxide region with consequences for the final distribution of the nanocrystal sizes and positions.

- A redistribution and partial loss of the implanted Ge was observed and addressed to the formation of volatile GeO. An enhanced diffusivity of Ge in SiO_2 was found and explained as an oxygen vacancy assisted process.

- A dissociation of as-grown and Si^+ implanted thin SiO_2 layers was found during annealing at temperatures of $T > 1100°C$ in Ar at ultra-low partial pressure of oxygen which is explained by the emanation of SiO.

- The Ge redistribution effect is advantageously used for the formation of a self-organized δ-like layer of Ge nanocrystals in vicinity to the Si/SiO_2 interface which is a desired configuration to achieve nanodot memory devices.

- An electrical model is developed based on a floating-gate-like approach to describe the transient programming and leakage current characteristics of NC containing thin oxides.

- The distribution of the tunneling oxide thickness between the near-interface Ge nanocrystals and the Si substrate is determined from simple programming characteristics using the electrical model.

- A comparison of measured with calculated current-voltage characteristics of NC containing thin gate oxides reveals that the leakage currents are strongly related to the location of the nanocrystals and not driven by ion implantation caused oxide defects.

Within this PhD thesis some previous published or submitted publications are included whereas their internal relation within this thesis is given as follows: The first publication [V. Beyer and J. v. Borany, Phys. Rev. B, 014107 (2008)] addresses the self-organized formation of a δ-layer of Ge nanocrystals in thin oxides by ion beam synthesis for the fabrication of nanodot memory devices. A transient electrical model is developed in the second publication [V. Beyer, J. v. Borany, and M. Klimenkov, J. Appl. Phys. 101, 094507 (2007)] to describe the programming behavior of such devices. In the third publication [V. Beyer, J. v. Borany, and M. Klimenkov, Appl. Phys. Lett. 89, 193505 (2006)] this model is used to determine the distribution of tunneling oxide thicknesses from electrial characteristics of such nanocrystal containing gate oxides. For such oxides also leakage current characteristics are modeled, calculated and compared to measured data which is the topic the publication [V. Beyer, J. v. Borany, M. Klimenkov, and T. Müller, submitted to J. Appl. Phys., 2009]. The samples were prepared under special annealing conditions, namely a low partial pressure of oxygen, to reduce a parasitic oxidation of the embedded nanocystals. However, under these conditions at elevated temperatures a dissociation of implanted and as-grown oxides was observed and is discussed in detail in [V. Beyer, J. v. Borany, and K.-H. Heinig, J. Appl. Phys. 101, 053516 (2007)].

Fundamentally, the author prepared these publications himself, especially regarding the content, the conception, the underlying experiments, calculations, interpretations and analysis. The contribution of the co-authors is related in case of Dr. J. von Borany as the advisor at FZD mainly to very worth- and fruitful discussions supporting in organizing and performing experiments which is gratefully acknowledged. Dr. K.-H. Heinig supported in discussions concerning the physics of described diffusion mechanisms and in KMLC simulations for Si irradiation. Dr. M. Klimenkov and Dr. T. Müller carried out all TEM investigations and the KLMC simulation for Si implanation in 20 nm thin gate oxides, respectively.

Zusammenfassung

Im Hinblick auf eine mögliche Anwendung als Nanocluster-Speicherbauelement wurden in 20 nm dünnen Gateoxiden (SiO_2) 1 - 3 nm große Ge and Si Nanocluster synthetisiert, und zwar mittels Niederenergie-Ionenimplantation und anschliessender Ausheilung. Abhängig von dem gewählten Ion (Ge oder Si), dessen Energie und Fluenz wurden die Nanocluster entweder nahe der Oxidmitte oder in einer sehr schmalen Bereich im Oxid nahe des darunterliegenden Silizium-Substrates hergestellt. Man benötigt hohe Ionenfluenzen, um eine hinreichende Übersättigung mit Fremdatomen zu erreichen und somit Nanocluster in Oxiden mittels Niederenergie-Ionenimplantation erzeugen zu können. Für die verläßliche Berechnung der entsprechenden Ionenprofile müssen dynamische Änderungen der SiO_2-Oxidzusammensetzung während der Implantation berücksichtigt werden, so z.B. das Anschwellen des Oxides durch den Materialeintrag oder der Sputter-bedingte Materialabtrag an der Oxidoberfläche. Die Implantationsparameter wurden so gewählt, dass die Profilmaxima etwa in der Oxidmitte zu liegen kommen bei gleichzeitig mäßiger Schädigung der Si/SiO_2 Grenzfläche bzw. des Si Substrates.

Im Falle flacher Implantation in dünne Oxide spielt die Umgebungsatmosphäre während des Waferhandlings, der Waferreinigung oder der Ausheiung eine deutlich zunehmende Rolle. Aus der Umgebungsluft können Feuchtekomponenten (H_2O, H^+, OH^-) in das geschädigte Oxid eindrigen, was oberflächennah im Oxid zu einer Anreicherung von Wasserstoff und Sauerstoff führen kann. Nach der Implantation wird ein Ausheilungsschritt benötigt, um das Wachstum der Nanocluster zu stimulieren und das geschädigte Oxid (und das Si Substrat) wiederherzustellen. Zur gleichen Zeit kann z.B. das implantierte Germanium mit dem Sauerstoff- bzw. Wasserstoffüberschuß des Oxides zu GeO_2 oxidieren oder zu flüchtigen Verbindungen wie z.B. zu GeH_4 or GeO reagieren. So beeinflußt der Ausheilungsprozeß bei der Ionenstrahlsynthese von Si und Ge Nanoclustern die Tiefenprofile der Elemente und die resultierende Nanoclusterverteilung auf unterschiedliche Art und Weise.

Nach Ge^+ Implantation und Ausheilung wird, begleitet von einem Ge-Verlust, eine deutliche Umverteilung des Ge im Oxid in Richtung des Si Substrates beobachtet. Dabei gewinnt Ge im Oxid eine um Größenordnungen höhere Diffusivität verglichen mit der, die für interstitielle Diffusion von Ge in SiO_2 bekannt ist. Die präsentierten Experimente zeigen, dass beide Effekte, die Umverteilung als auch der Verlust, mit der Bildung von sehr beweglichen GeO Molekülen verbunden ist. Der Verlust entsteht, wenn ein diffundierendes GeO Molekül an die SiO_2 Oberfläche gelangt und dort an die Ausheilatmosphäre abgegeben wird. Befindet sich ein GeO Molekül im Oxid, kann man sich dieses auch eingebunden in das SiO_2-Netzwerk als einen Ge-basierten Sauerstoffmangeldefekt im Oxid vorstellen. Dabei kann der Diffusionsmechanismus als ein korrelierter Bewegungsprozess des eingebundenen Germaniumatoms mit einer Sauerstoffvakanz beschrieben werden. Es

könnte sich also bei der erhöhte Diffusivität des Ge in SiO_2 um einen Sauerstoffvakanz-unterstützten Prozess handeln.

Im Falle der Si^+ Implantation entstehen die Si Nanocluster im Wesentlichen in der Mitte des Oxides ohne derartig signifikante Umverteilungsprozesse aufzuweisen. Die eindrigende Feuchte oxidiert den enstandenen Si Überschuss im Oxid nahe der Oxidoberfläche zu SiO_2. Um den Einfluß der Oxidanten aus der Ausheilatmosphäre zu begrenzen, wurde für die Temperaturbehandlung ein Kurzausheilschritt gewählt, der in Neutralgasatmosphäre bei äußerst geringem Sauerstoffpartialdruck durchgeführt wurde. Allerdings hat das zur Folge, dass bei Temperaturen von $T > 1100°C$ - welche weit über denen liegen, die man Synthese von Si or Ge Nanoclustern benötigt (950 - 1050°C) - eine Dissoziation der Si^+-implanterten und auch der unimplantierten dünnen SiO_2 Filme auftritt. Diese Auflösung des Oxides wird durch das Ausgasen von SiO-Molekülen erklärt.

Der Effekt der Ge Umverteilung wird hier vorteilhaft ausgenutzt, indem gezielt eine δ-Schicht an Ge Nanoclustern in nächster Nähe zur Si/SiO_2 Grenzfläche selbstorganisierend erzeugt wurde. Dabei handelt es sich um eine gewünschte Anordnung für Nanocluster-basierte Speicherbauelemente, bei denen kleine Programmierspannungen und kurze Programmierzeiten realisiert werden sollen. Die Erzeugung von Nanoclustern in nächster Nähe zur Si/SiO_2 Grenzfläche wird durch parasitäres Mischen dieser Grenzflächen ermöglicht, falls die Stoßkaskaden der implantierten Ge^+ Ionen das Si Substrat erreichen. Während der Temperung wird die Grenzfläche thermisch aktiviert wiederhergestellt, wobei kleine Si Präzipitate im Oxid verbleiben. Diffundierende Ge Atome (bzw. GeO Moleküle) aus dem Inneren des Oxides kondensieren an diesen Si Clustern, sammeln sich dort und wachsen weiter zu Ge Nanoclustern. Dabei werden die anfänglichen Si Präzipitate durch den Sauerstoff, der durch die eingefangenen GeO Molekülen zur Verfügung gestellt wird, oxidiert. Die Ge Nanocluster entstehen dort in einer Größe von etwa 2 nm in einer sehr hohen Flächendichte von etwa $3 \times 10^{12}\,cm^{-2}$.

Darüber hinaus wurde basierend auf einem Floating-Gate-Ansatz ein elektrisches Modell zur Beschreibung des transienten Programmierverhaltens Nanocluster-haltiger dünner Gateoxide entwickelt. Dabei wird angenommen, dass der Landungstransfer vom Si Substrat zu der Ge Nanoclusterschicht durch direktes Tunneln geschieht. Quantenconfinement und Coulombblockadeeffekte kleiner Ge Nanokristalle (1 - 6 nm) werden diskutiert, können aber für die vorliegenden Strukturen als vernachlässigbar angesehen werden. Eine deutliche Übereinstimmung des berechneten Programmierverhaltens mit den experimentellen Daten, die an Metall-Oxid-Halbleiter Kapazitätststrukturen gewonnen wurden, bestätigt die Gültigkeit des Modells. Es wird gezeigt, dass das Programmierverhalten der Nanodot-Speicher im Wesentlichen von der Tunneldistanz zwischen den Nanokristallen und dem Si Substrat anhängt. Unter Berücksichtigung dieses Modells gelang es erstmals, eine Verteilung der Tunneloxiddicken d_{tox} aus gemessenen Programmierkurven zu bestimmen und zwar mit recht hoher Genauigkeit, wie Bilder aus Transmissionselektronenmikroskopiemessungen zeigen (aufgenommen im "high-angle annular dark-field" Modus). Die Änderung von d_{tox} während der Temperaturbehandlung wird anhand von Ostwald-Reifen diskutiert, wobei d_{tox} mit fortschreitender Ausheilzeit anwächst. Zur Beschreibung von Leckströmen durch Nancluster-haltiger Oxide wur-

den Strom-Spannungs-Charakteristika elektrisch modelliert und berechnet, und zwar für Gate-Oxide, die Si oder Ge Nanocluster in unterscheidlicher Verteilung, Größe und Flächendichte enthalten. Die dafür benötigten Strukturinformationen wurden aus Transmissionselektronenmikroskopiedaten gewonnen. Die berechneten Stromtransfercharakteristika weisen wesentliche Übereinstimmungen mit den entsprechenden Meßdaten auf. Messungen, bei denen gleichzeitig Strom und Kapazitätsdaten aufgenommen wurden, bestätigen, dass die elektrischen Felder innerhalb des Oxides durch die örtliche Verteilung geladener Cluster bestimmt sind. Nach Ionenimplantation und anschließender Ausheilung hängen die Leckströme durch die hier untersuchten clusterhaltigen dünnen Gateoxide im Wesentlichen von der Lage der Nanocluster ab und werden nicht durch implantationsbedingte Oxiddefekte bestimmt.

Insbesondere für die Ge Nanocluster-haltigen Oxiden lassen sich kurze Programmierzeiten und geringe Programmierspannungen realisieren, allerdings bei nur kurzer Ladungshaltung. Somit zeigen die hergestellten Si und Ge Nanocluster-haltigen Speicherbauelemente eher ein Verhalten eines flüchtigen Speichers (DRAM) bzw. ein quasi-nichtflüchtiges Speicherverhalten. Als nichtflüchtige Speicher sind diese Bauelemente daher nicht oder nur bedingt verwendbar.

Im Folgenden sind die wesentlichen Ergebnisse nochmals zusammengefasst:

- Sehr kleine Ge and Si Nanokristalle wurden in dünnen Gateoxiden mittels Ionenstrahlsynthese hergestellt, wobei als Anwendung ein Nanopunkt-Speicherbauelement im Fokus stand.

- Es wurde festgestellt, dass bei hohen Fluenzen und geringe Implantationsenergien dynamische Änderungen der Oxidzusammensetzung, wie z.B. das Anschwellen des Oxides oder der sputterbedingte Abtrag der Oxidoberfläche, für eine verlässliche Bestimmung von Ionenimplantationsprofilen berücksichtigt werden müssen.

- Während der Lagerung an Luft oder während der Reinigungs- bzw. Ausheilprozeduren dringt Feuchtigkeit in das geschädigte Oxid oberflächennah ein und führt dort zu einer Erhöhung des Wasserstoff und Sauerstoffgehaltes. Dies hat wiederum Konsequenzen für die Lage- und Größenverteilung der im Oxid erzeugten Nanokristalle.

- Sowohl eine Umverteilung als auch ein teilweiser Verlust des implantierten Germaniums wurde beobachtet und mit der Bildung von flüchtigem Germaniummonoxid (GeO) begründet. Ebenso wurde eine erhöhte Diffusivität von Ge in SiO_2 gefunden, die hier als ein Sauerstoffvakanz-unterstützter Prozess erklärt wird.

- Während der Ausheilung der Oxide in Argon bei gleichzeitig besonders niedrigem Sauerstoffpartialdruck bei Temperaturen von $T > 1100°C$ tritt eine Dissoziation der thermisch gewachsenen implantierten und nicht-implantierten dünnen Siliziumoxide (SiO_2) auf und zwar verursacht durch die Bildung von flüchtigem Siliziummonoxid (SiO).

- Der Effekt der Ge Umverteilung wurde vorteilhaft genutzt, um selbstorganisiert eine dünne Schicht an Ge Nanokristallen mit einer sehr schmalen Verteilung im

Oxid nahe der Si/SiO_2 Grenzfläche zu erzeugen. Dabei handelt es sich um eine Anordnung, wie sie für Nanopunkt-Speicherbauelemente gewünscht wird.

- Basierend auf der "Floating-Gate"-Näherung wurde ein elektrisches Modell für die Beschreibung des transienten Programmier- und Leckstromverhaltens dünner Nanocluster-haltiger Oxide entwickelt.

- Mithilfe dieses Modells gelang es erstmals die Verteilung der Tunneloxiddicken zwischen den grenzflächennahe Ge Nanoclustern und dem Si Substrat aus einfachen Programmiercharakteristika zu bestimmen.

- Ein Vergleich von gemessenen und gerechneten Strom-Spannungskennlinien Nanocluster-haltiger dünner Gateoxide zeigt, dass die Leckströme im Wesentlichen von der Lage der Nanocluster abhängen und nicht durch ionenimplantationsbedingte Oxiddefekte bestimmt sind.

Der inhaltliche Zusammenhang der enthaltenen Publikationen ergibt sich wie folgt: In der ersten Publikation [V. Beyer and J. v. Borany, Phys. Rev. B, 014107 (2008)] wird die selbstorganisierte Bildung von Ge Nanoclustern beschrieben, wie sie während deren Ionenstrahlsynthese in dünnen Gateoxiden zu beobachten ist. Dabei ist deren schmale Ortsverteilung ein wichtiges Kritierium für die Nutzung als Nanodot-Speicherbauelement. In der zweiten Publikation [V. Beyer, J. v. Borany, and M. Klimenkov, J. Appl. Phys. 101, 094507 (2007)] wird ein transientes elektrisches Modell für die Beschreibung des Programmierverhalten solcher Bauelemente entwickelt. Dieses Modell wird in der dritten Veröffentlichung [V. Beyer, J. v. Borany, and M. Klimenkov, Appl. Phys. Lett. 89, 193505 (2006)] dafür verwendet, die Verteilung der Tunneloxiddicken aus elektrischen Kennlinien Nanocluster-haltiger Gateoxide zu bestimmen. Für solche Oxide wurden auch Leckstrom-Charakteristika modelliert, berechnet und mit Meßdaten verglichen [V. Beyer, J. v. Borany, M. Klimenkov, and T. Müller, eingereicht bei J. Appl. Phys., 2009]. Die hier diskutierten Proben wurden unter besonderen Ausheilbedingungen hergestellt, nämlich bei sehr geringen Sauerstoffpartialdruck, um die parasitäre Oxidation der eingebetteten Nanocluster zu unterdrücken. Unter diesen Bedingungen aber höheren Ausheiltemperaturen ($T > 1100°C$) konnte eine Dissoziation der implantierten und thermisch erzeugten Gateoxide festgestellt werden, die in [V. Beyer, J. v. Borany, and K.-H. Heinig, J. Appl. Phys. 101, 053516 (2007)] detailliert diskutiert wird.

Der Verfasser hat diese Publikationen inhaltlich selbstständig konzipiert, erarbeitet und verfasst, sowie die zugrunde liegendenden Experimente, Berechungen, Messungen und Auswertung im Wesentlichen selbst durchgeführt. Die Mitarbeit der genannten Mitautoren lag im Falle von Herrn Dr. J. von Borany als fachlichem Betreuer am FZD insbesondere in der sehr wertvollen fachlichen Diskussion und der Unterstützung bei der Durchführung von Experimenten. Fachlichen Diskussionen mit Herrn Dr. K.-H. Heinig waren sehr hilfreich insbesondere hinsichtlich der beschriebenen Diffusionsmechanismen und KMLC Simulationen für den Fall der Si Durchstrahlung. Dr. M. Klimenkov unterstütze bei der Erzeugung und Interpretation der gezeigten TEM Bilder und Dr. T. Müller führte die KLMC Simulation für die Si-implantierten Gateoxide durch.

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